Master's Thesis

Design of Low Footprint -40º C to 110º C Bandgap References in 40 nm Technology





Master in Microelectronics: Design and applications of Micro/Nano-scale Systems

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SUMMARY OF THE THESIS

This thesis addresses the design and implementation of bandgap voltage references, which are essential components of integrated circuits, and describes a design instance for a CMOS 40 nm technology. The work is motivated by the need for stable and reliable reference voltages in mixed-signal systems, which are crucial for correctly operating the various analog and digital components. Specifically, the bandgap reference in this thesis has been conceived for asynchronous image sensors designed according to the dynamic vision sensor concept.

KEY COMPONENTS AND THEIR ROLES

The first chapter describes the working principles of bandgap references and provides an overview of various architectures. These circuits leverage the temperature-dependent properties of silicon to create a voltage that remains stable across a wide range of temperatures. The thesis explains the underlying physics, including PTAT (Proportional to Absolute Temperature) and CTAT (Complementary to Absolute Temperature) voltages, and how combining these can produce a temperature-independent reference voltage.

Several bandgap architectures are included in the overview, highlighting their evolution and the trade-offs involved:

- Widlar's Bandgap Reference: the pioneering topology which introduced the fundamental concepts of bandgap references.
- Kujik's Implementation: a more refined design addressing some of Widlar's limitations, such as temperature-dependent currents.
- Standard Voltage Bandgap Reference: a widely used design that balances performance and complexity, suitable for many applications.
- Low-Voltage Bandgap Reference: designed for modern, deep sub-micron technologies where supply voltages are lower than provided by conventional bandgap references.

DEVELOPMENT OF DESIGN EQUATIONS:

The second chapter compiles design equations derived by using models that capture the main second-order effects that deteriorate the circuit's performance, mainly:

- Circuit Stability
- Power supply rejection
- Noise

DESIGN AND IMPLEMENTATION

The third chapter covers the design and implementation process for a standard bandgap reference in 40 nm technology. Key aspects of this process include:

- Schematic Design: Using parameter scaling and g_m/I_d methodology to size components correctly.

- Amplifier Design: Ensuring the necessary gain and stability for the reference circuit.
- Start-Up Circuit: Implementing mechanisms to ensure the circuit begins operating correctly upon power-up.
- Layout Design: Addressing challenges in physical implementation to minimize parasitics and ensure robust performance.

SIMULATION AND RESULTS

The final chapter includes simulations to validate the design and provide insight on key performance metrics such as:

- Stability: ensuring the reference voltage remains constant under varying conditions.
- Power Supply Rejection (PSR): measuring the circuit's ability to reject noise from the power supply.
- Noise Performance: identifying sources of noise within the circuit.

The validation results demonstrate that the designed bandgap reference meets the desired specifications, with good temperature stability, suitable for integration into advanced mixed-signal systems. This is achieved with a very low area-consumption.

As this circuit is being integrated in a chip, future work will also include measurement and performance evaluation in real-world implementation.

In summary, this thesis presents the design and implementation of a crucial circuit component for systems-on-chip, from specification and architecture selection to schematic and layout design. Validation using computer-aided software supports its functionality for fabrication, thus traversing a complete design flow and reinforcing the knowledge gained during the master's program.

Summary

CHAPTER 1- INTRODUCTION

This thesis reports the design of a bandgap voltage reference in a CMOS 40 nm technology. This circuit is intended as part of two integrated circuits implementing event-based sensors designed in the same technology in the framework of an European Defense Fund (EDF) project. Due to confidentiality constraints imposed by the project itself and the foundry in charge of fabrication, details concerning technology parameters cannot be disclosed. This constraint mainly affects Chapter 4. This chapter overviews basic concepts and architectures for voltage references and, more specifically, bandgap references - an essential component for integrated circuits since it was devised in the late 1960s [1]. This overview revision ends by selecting a specific architecture for implementation.

1.1 MOTIVATION

1.1.1 COMMON MIXED SIGNAL CIRCUIT STRUCTURE

Mixed-signal systems embed different functional blocks, each handling different kinds of signals and implementing different dedicated functions such as signal conditioning, analog-to-digital conversion, power management, etc. Particularly, voltage and current references are crucial components as they set the bias conditions of amplification devices and define the dynamic ranges of analog-to-digital converters, among other critical functions.

It is well known that biasing determines the behavioral features of any amplifier, including the gain, the terminal impedances, the non-linearity, distortion, the frequency response, and the noise. References must be generated on-chip, using dedicated circuits intended for this purpose, to guarantee correct operation and PVT robustness. Figure 1 illustrates the concept of embedded reference generation [2]. While on-chip reference generation is advisable for any circuit, it becomes a must in the case of Systems-on-Chip as those targeted the framework of this project.

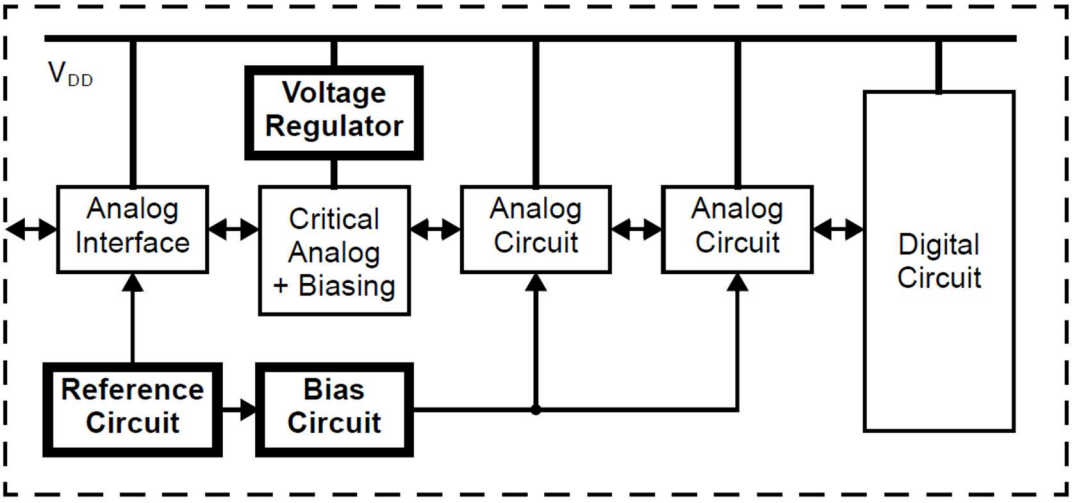


Figure 1. BLOCK DIAGRAM OF GENERAL MIXED SIGNAL CIRCUIT [2]

Figure 1 shows a general mixed signal system with different analog and digital blocks that are not specified, and surrounded by a thicker box, we have the three main signal generator blocks needed for the correct system functioning. The blocks are a reference circuit, to generate fixed valued voltages or currents, a biasing circuit to ensure proper operating point of active devices in the circuit, and finally a voltage regulator to reduce noise and variations of power [3].

1.1.2 BASIC ANALOG BLOCKS

We will now take a deeper look at each of these blocks and introduce their main functions and design challenges.

1.1.2.1 BIAS CIRCUIT

This circuitry has a main objective of positioning all transistors in the correct operating point. This is needed in all circuits in general, and biasing can be done either in voltage-mode or a in current-mode. Unlike references, these voltages or currents need not be fixed but should vary with process and temperature to ensure devices stay well biased [2].

An example of a biasing need is the current biasing of a transconductance amplifier. Such as the one we see in 0.

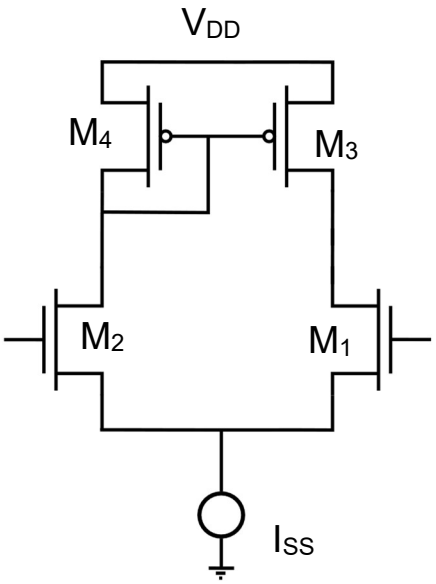


Figure 2. 5 TRANSISTOR OTA WITH BIASING

We see that the four transistors (a differential pair and a current mirror) are biased by a current I_{SS}. This can be achieved by mirroring a current with a simple current mirror, substituting the current source by a transistor whose gate voltage will be the biasing in this case.

Challenges arise when the original bias current is generated far away in the physical circuit and must be precisely mirrored. Adding a long connection to carry bias voltages can result in perturbations due to coupling, variations of the properties of the substrate, and variations of transistor threshold voltages due to on-chip variations. In this case, a solution would be to use a current mode bias to take the current to a transistor near the objective and then mirror it, diminishing variations [2].

We also want to make sure biasing circuits are as area-efficient as possible, as they are auxiliary circuits and designers need space for the rest of the circuit to perform complex operations. This is why bias circuits are usually shared between various blocks [3].

1.1.2.2 VOLTAGE REGULATORS

These circuit blocks are needed to supply critical analog systems with a voltage supply with low noise [4]. This is greatly important in mixed signal applications as digital circuitry introduces a great amount of noise to supplies that can interfere with analog circuitry's operation.

They are usually built using a feedback configuration built around a high open loop gain opamp, thus generating a low noise DC voltage that closely tracks a reference value [3] – see Figure 3. In this design, we have to be careful with poles positions, as internal amplifier's pole and the external load pole have to be positioned in such a way that the system is stable. The output of this system is $V_o = V_{ref}(1 + R_B/R_A)$ assuming that the virtual ground constraint holds exactly.

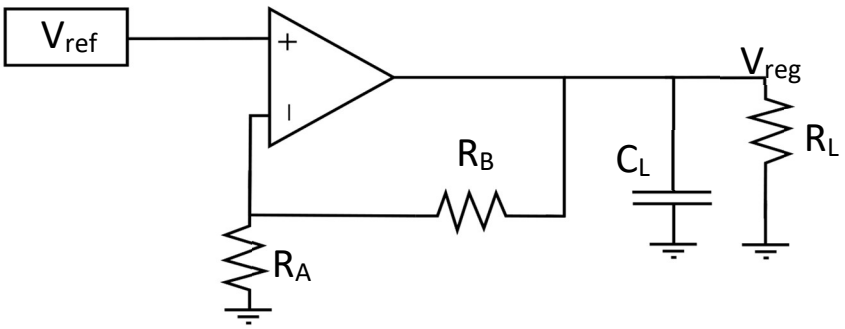


Figure 3. VOLTAGE REGULATOR SCHEMATIC [4]

One of the main issues to consider is the voltage drop produced by the voltage regulator which will reduce the available voltage range [2]. This can be overcome by using a circuit like the one in Figure 4. In this case, due to the virtual ground principle in the amplifier, the reference voltage is copied to the output directly, without dropout ideally. The polarity of feedback inputs is reversed as the PMOS transistor adds a negative sign and we get negative feedback through the positive input this way. In this case, stability is also crucial, and the system can be studied

like a two-stage amplifier by considering the PMOS as the second stage. We can also obtain a current from this design.

Disadvantages of this design include the low supply rejection ratio of the PMOS transistors, another equivalent design can be done with NMOS transistors which provide a higher supply rejection, but these also produce a higher dropout voltage [2],[4].

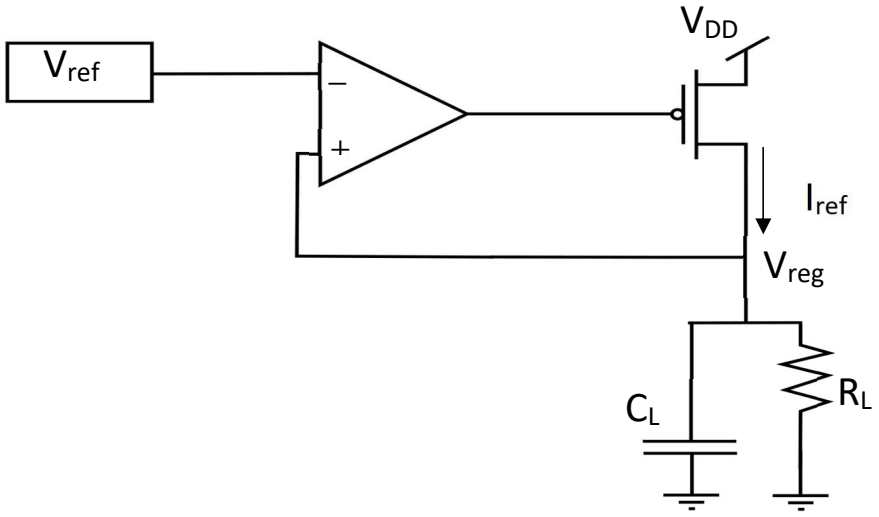


Figure 4. LOW DROPOUT VOLTAGE REGULATOR [2]

1.1.2.3 REFERENCE CIRCUITS

Finally, we have reference circuits. These circuits are envisioned to generate a fixed value voltage reference for the rest of the system. Hence, these references need to be not only fixed in time but also under process and temperature variations. They can be used to generate biasing current, reference voltages for comparators, or in interfaces between two integrated circuits [2].

It is for this reason that a quantity that stays invariant along several different circuits must be found so that it serves as reference. There are little quantities with properties as this in the realm of CMOS circuitry as they are usually heavily reliant on properties such as doping, temperature, areas. One quantity that stays invariant in all cases is what's known as the Silicon's bandgap, this is the energy between valence and conduction bands in Silicon.

Most of reference circuits are designed using this constant to obtain an invariant voltage reference with a circuit that is a Bandgap Voltage reference. Next sections briefly overview their working principles are the basic guidelines to design them.

1.2 BANDGAP REFERENCE WORKING PRINCIPLES

Semiconductor circuits do not offer a quantity that is invariant of ambient temperature directly and this circumstance represents a significant issue for electronic design. A solution for this issue in the design of resistors we can use a well-refined series combination of directly proportional to temperature resistors and inversely proportional to temperature resistors, which cancel correctly their dependences with temperature. But in the case of voltages and currents, and not physical properties like conductance this mission gets more difficult [1].

The working principle of a temperature-invariant voltage reference circuit is the same as the resistors described above. We need to find a voltage with a positive temperature coefficient (PTAT - proportional to absolute temperature) and a voltage with a negative temperature coefficient (CTAT – Complimentary to absolute temperature). By combining both these quantities we would obtain a temperature-independent voltage.

1.2.1 CTAT VOLTAGE PRINCIPLE

It is easy to find a CTAT voltage in basic electronic devices. We just must go to the Shockley equation (1) [5].

$$\boldsymbol{I = I_s\left(e^{\frac{V}{U_T}} - 1\right)} \tag{1}$$

where $\mathrm{I_s}$ is the saturation current of the diode, and $\mathrm{U_T}$ the thermal voltage which is defined as:

$$\boldsymbol{U_T = \frac{k_B T}{q}} \tag{2}$$

Where k_B is the Botzmann constant, T is the absolute temperature, and q is the electron charge. Calculating the derivative of previous equation with respect to temperature we can obtain the temperature coefficient, which requires accounting for the temperature dependence, which can be formulated as [5]:

$$\boldsymbol{I_s = qAn_i^2\left[\frac{D_p}{(W_{ln} - W_n)N_d} + \frac{D_n}{|W_{lp} - W_p| \cdot N_a}\right]} \tag{3}$$

This equation includes several constants of the p-n junction, $\mathrm{D_p}$ and $\mathrm{D_n}$ are the diffusion coefficients for holes and electrons respectively, $(W_{ln} - W_n)$ and $|W_{lp} - W_p|$ the lengths of the neutral zones of the junction and $\mathrm{N_a}$and $\mathrm{N_d}$ are the doping concentrations of p and n zones. An important factor here is $\mathrm{n_i}$, the intrinsic carrier concentration, which is fully dependent on temperature following equation (4) [4].

$$\boldsymbol{n_i = B^* \cdot T^{\frac{3}{2}} \cdot e^{-\frac{E_g}{2k_bT}}} \quad (4)$$

where B^* is a constant depending on effective carrier's masses and fundamental constants and $\mathrm{E_g}$ is the bandgap energy. Regarding the diffusion coefficients they can be assessed taking into account that:

$$\boldsymbol{D \propto \mu(T) \cdot T = \mu_o T^m \cdot T} \quad (5)$$

Assuming all the rest of the constants are invariant with temperature, we will now derive an expression for the diode's voltage temperature coefficient. We have that

$$\boldsymbol{I_s = A^* B^* \cdot T^{4+m} e^{-\frac{E_g}{kT}}} \quad (6)$$

where A^* contains all the constants in the previous expressions to simplify calculations. Operating with previous equations we arrive at the expression for the voltage temperature coefficient:

$$\boldsymbol{\frac{\partial V}{\partial T} = \frac{V - (3+m)U_T - E_g/k}{T}} \quad (7)$$

where $m \approx -3/2$ [6]. We can evaluate this expression and we find it is a negative value at room temperature of 300K [4]. Thus, this can be used as a CTAT voltage generator, we are left with the PTAT voltage.

1.2.2 PTAT VOLTAGE PRINCIPLE

In 1965, Widlar [7] observed that the difference in Base-Emitter voltage of two BJT transistors biased with two different current densities produces a PTAT voltage. This can easily be seen with two diode-connected transistors with different areas.

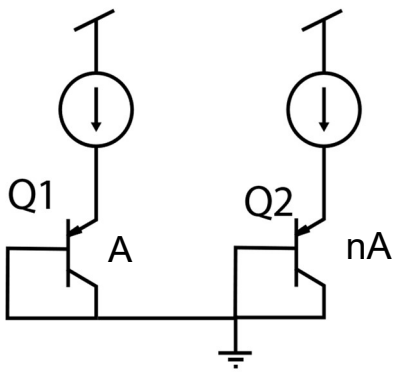


Figure 5. DIODE CONNECTED BJT TRANSISTORS WITH DIFFERENT AREAS

Transistors Q1 and Q2 in Figure 5 fit to the following expression:

$$\boldsymbol{I = I_D\left(e^{\frac{V_{BE}}{U_T}} - 1\right) \approx I_D e^{V_{BE}/U_T}} \quad (8)$$

where I_D is, in this case, proportional to the area of the junction and is of the form $I_D \propto B \cdot A$, with B a constant that unites all variables of the technology and A the area. If both are designed in the same chip, they will have equal B. Biasing both with the same current we will have that:

$$\boldsymbol{\Delta V_{BE} = V_{BE2} - V_{BE1} = U_T \log\left(\frac{I}{I_{D2}}\right) - U_T \log\left(\frac{I}{I_{D1}}\right) = U_T \log\left(\frac{nA}{A}\right)} \quad (9)$$

As we can see, this difference of voltages only depends on temperature by the factor U_T, which makes it increase linearly with temperature with a slope $\frac{k}{q}\log n$.

Now we have all the foundations set to obtain a voltage with a null temperature coefficient. The only thing left to do is find a way to join these two values. We will then have $V_T = V_{BE} + C \cdot \Delta V_{BE}$ with C a convenient scaling constant, this has a temperature dependance given by the next expression.

$$\boldsymbol{\frac{\partial V}{\partial T} = \frac{V - (3+m)U_T - \frac{E_g}{k}}{T} + C \cdot \frac{k}{q}} \quad (10)$$

As the CTAT voltage has a different curvature than the PTAT voltage (which has no curvature) they will only compensate each other at one temperature, which is usually the design temperature of the intended application. Now we only have to find a way to translate this into a design that achieves this sum of voltages – described in the next section.

1.2 REVIEW OF EXISTING BANDGAP ARCHITECTURES

In this section, we will now revise some of the main architectures that exist for bandgap references. We will study how they achieve the principles showed in the previous section and how they differ from one another. We will start with the first implementation of a Bandgap voltage reference.

1.2.1 WIDLAR'S BANDGAP REFERENCE GENERATOR [8]

In 1971 Widlar [8] followed his ideas presented for the PTAT voltage and designed the first bandgap voltage reference using these ideas. We can see the implementation in Figure 6. It is based on the ideas presented before. In node A we have the voltage V_{BE1}, while in node B, we have the voltage $V_{BE1} - V_{BE} =$

$\Delta V_{BE(1-2)}$. In node C we then have V_{BE3}, and finally through ohms law we find that $V_D = V_{BE3} + \frac{R_4}{R_3}\Delta V_{BE1-2}$.

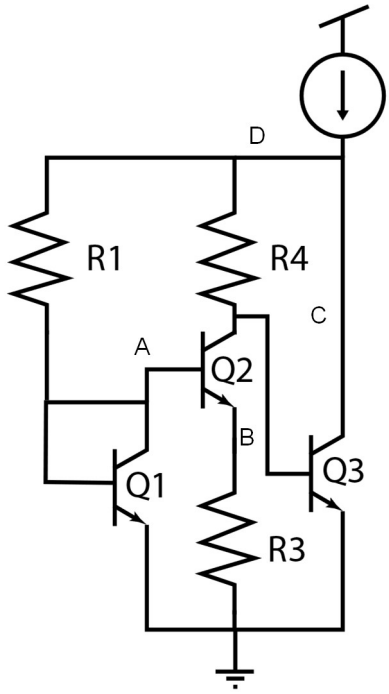


Figure 6. WIDLAR'S VOLTAGE REFERENCE

This circuit implements the general form of independent to temperature voltage we described in the previous section through transistors and resistors. It is a low noise source, and its precision depends on mismatch that can be achieved in a high degree. The most important variable here which is the base emitter voltage in npn transistors is one of the best understood and predictable [8].

This first implementation was soon found to have some issues. The main one being that this equation developed for the output voltage circuit is obtained neglecting the base currents of transistors, which have a big effect, as the variability of the currents and the effect of temperature on the forward current gain of common emitter configuration of BJT introduces a voltage error and drift as was remarked by Brookaw in [9].

1.2.2 KUJIK'S VOLTAGE BANDGAP REFERENCE

The circuit (Figure 7) proposed by Kujik in the paper [10], based on the ideas of Brookaw in [9], is a commonly employed bandgap implementation found in virtually any book about CMOS circuit design.

Node "a" in Figure 7 has a voltage V_{BE1}, while at node "b" we have V_{BE} ; assuming that the opamp DC gain is large enough, the virtual ground constraint applies thus ensuring that nodes "a" and "c" have practically the same voltage.

Hence, the voltage drop at R_2 is $\Delta V_{BE} = V_{BE1} - V_{BE2}$, and the current flowing through the negative feedback resistor is $I = \Delta V_{BE}/R_2$ thus yielding the following output voltage:

$$V_{out} = V_{BE1} + \frac{R_1}{R_2}\Delta V_{BE} \tag{11}$$

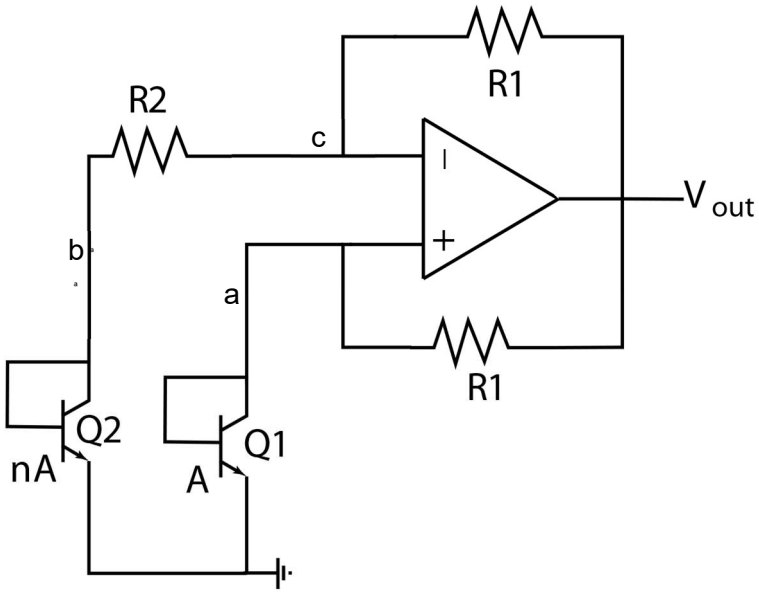


Figure 7. KUJIKS' BANDGAP IMPLEMENTATION

Equation (11) includes the intended combination of V_{BE} and ΔV_{BE} that supports obtaining a temperature independent voltage. However, there are some drawbacks that deserve consideration for practical design [1]:

- We have assumed that both branch currents are constant and equal because feedback resistances, R_1, are also equal. Nevertheless, there are mismatches and BJT currents are not constant and are temperature dependent, which affect the results and require adjustments.
- Because the circuit has negative and positive feedback loops, stability issues may arise that require dedicated analysis to prevent instabilities.
- Implementing *npn* transistors with the configuration needed might not be possible as an option in CMOS.

1.2.3 STANDARD VOLTAGE BANDGAP REFERENCE

The circuit in this section overcomes some of the issues of the previous circuit. It is a standard voltage reference, called this way because of the value of the voltage generated. Figure 8 shows the circuit.

This implementation is quite similar to that reported in [11]. This circuit includes two currents targeted for same value flowing through two different branches. Excluding virtual ground deviations, current equality is guaranteed by

construction (transistors have the same terminal voltages) provided branches are matched. Indeed, the principle is similar to that of the two branches in the previous circuit but now biasing currents are generated by CMOS-controlled current sources, fixing the issue of PTAT dependence of BJT-generated currents.

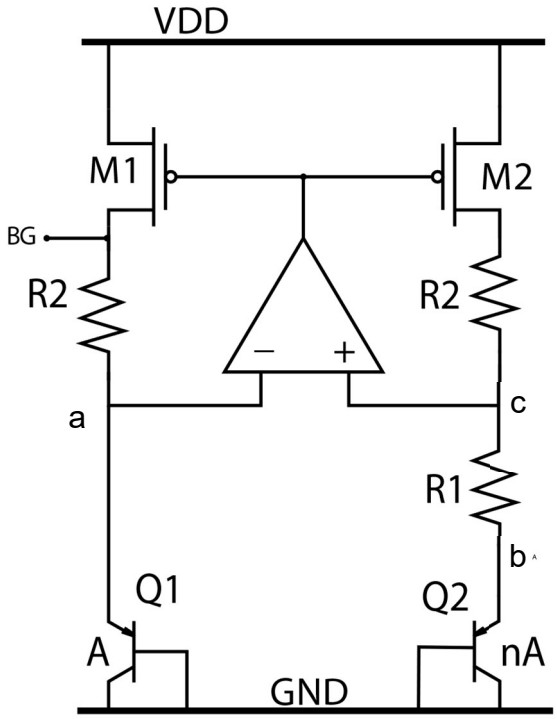


Figure 8. STANDARD VOLTAGE BANDGAP REFERENCE

Note that node "a" has a voltage V_{BE1}, and node "b" a voltage V_{BE2}. Due to virtual ground constraint, voltages at "a" and "c" are the same. This way the voltage drop in R_1 is $\Delta V_{BE} = V_{BE1} - V_{BE2} = U_T \log n$. And the current is:

$$\boldsymbol{I_{branch} = \frac{\Delta V_{BE}}{R_1} = \frac{U_T \log n}{R_1}} \tag{12}$$

After some calculations, the voltage at node BG is:

$$\boldsymbol{V_{BG} = V_{BE1} + R_2 I_{branch} = V_{BE1} + \frac{R_2}{R_1} U_T \log n} \tag{13}$$

As already said, similar working principle than Figure 7, but now with two CMOS controlled current sources.

We can here adjust R_2/R_1 in the design to ensure that temperature coefficient is compensated correctly. According to equation (7) we can obtain the value for the negative temperature coefficient, which using some common values for CMOS technology turns out to be $\partial V_{BE}/\partial T \approx -1.5mV/K$ at 300K and with $V_{BE} \approx 750mV$ [4], by choosing $\frac{R_2 k}{R_1 q} \log n = 1.5mV/K$ we now cancel out the temperature

dependence, and at 300K, we will obtain a standard reference voltage of $V_{BG} = 1.24V$.

Although this circuit can support quite a functional design, it has some drawbacks [1], namely:

- Transistors and amplifiers introduce flicker noise, to reduce it, a large transistor must be chosen.
- It can exhibit a low power supply rejection ratio
- With a 0 mA current in both branches the circuit is at equilibrium and will not generate any voltage. To solve this a start-up circuit must be designed. (For an implementation see section 3.3)
- Amplifier's feedback loop stability still has to be accounted for.

1.2.4 Low-Voltage Bandgap Reference

As we have seen, in the previous design we found that the voltage generated is fixed to a value of 1.2V. This is not a problem in technologies with high supply voltages, but as we move on to lower technological nodes supply voltages are reduced below this reference. This created the necessity for a low-voltage reference that can fit in these designs. A common low voltage reference design is just a small variation of the previous bandgap and can be found in many books, such as [2], and we see it in Figure 9.

In this design, we apply the same working principle based on the virtual ground, in which in node "a" we generate voltage V_{BE1} CTAT, and the voltage drop in R_1 is $\Delta V_{BE} = V_{BE1} - V_{BE2}$, a PTAT voltage., but now we don't have resistance R_2 in series at Q1 branch to generate the bandgap voltage through it. Instead, we have current flowing through R_1 to be

$$\boldsymbol{I_{R1} = \frac{\Delta V_{BE}}{R_1} = \frac{U_T \log n}{R_1}} \quad (14)$$

Regarding R_2 , virtual ground sets a voltage drop of value V_{BE1}, forcing a current:

$$\boldsymbol{I_{R2} = \frac{V_{BE1}}{R_2}} \quad (15)$$

As there is no current flowing through the input of the amplifier, the current flowing through the transistor M2 is given by the expression:

$$\boldsymbol{I_{M2} = \frac{V_{BE1}}{R_2} + \frac{U_T \log n}{R_1}} \quad (16)$$

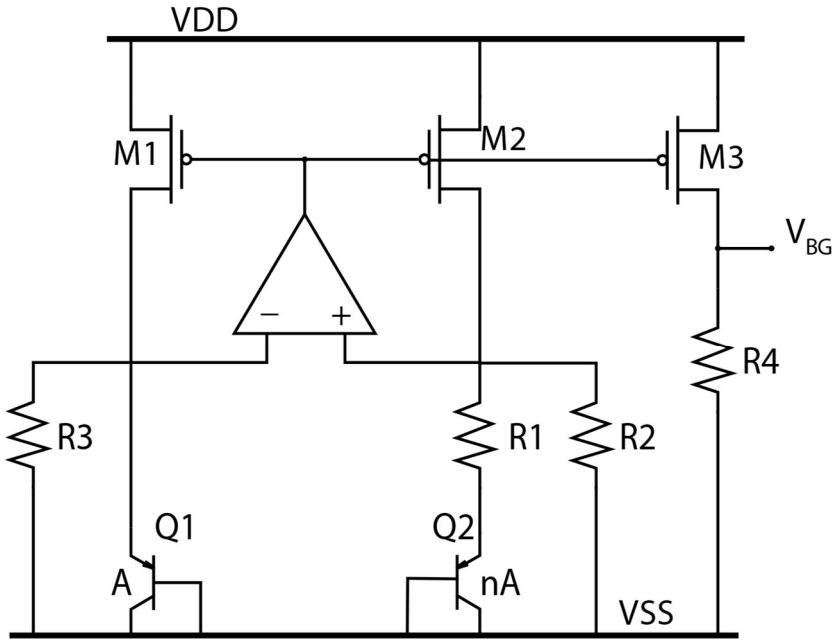


Figure 9. LOW -VOLTAGE BANDGAP REFERENCE

Which has the same form as the temperature-independent voltage, thus giving a temperature-independent current. As M_1 and M_2 are controlled current sources controlled by the voltage at gate, current at M_1 is the same as in M_2. Now if what we need is a temperature-independent current reference, we just have to mirror it, which is done with transistor M_3 implementing another controlled current source that mirrors the other two. Finally, voltage is generated by adding a resistance which whose value will adjust bandgap's output voltage.

Issues seen in the previous bandgap design persist in this design as it is just a small variation from it, but now to consider this design we have to account for the MOS transistor operating region. For the mirror in M_3 to work correctly it needs to operate in the saturation region, thus limiting the maximum value of the bandgap reference to

$$\boldsymbol{V_{BG(\max)} = V_{DD} - V_{dsatM3}} \quad (17)$$

This problem worsens at low temperatures as the bipolar temperature coefficient is -1.5mV, thus V_{BE} will increase leaving even less range to the transistors. This issue is especially significant in newer technologies as the voltage range is initially very reduced.

CHAPTER 2- STANDARD VOLTAGE BANDGAP REFERENCE

Based on the brief overview regarding bandgap voltage reference implementations completed in Chapter 1, this chapter addresses:

- Selecting the implementations that best fit the targeted application. In this case, the application is a voltage reference for comparators that trigger asynchronous image sensors. It will also serve as a bias for these circuits. In this implementation temperature independence is critical as these sensors will be used in environments with high temperature variations.
- Develop design equations for the most relevant second-order phenomena impacting of the circuit performance.

2.1 LOW VS. STANDARD VOLTAGE IMPLEMENTATION

The so-called low-voltage and standard-voltage implementations both correct the temperature dependence of BJT currents in Kujik's bandgap concept (see Figure 7) and share similar design issues. A priori, low-voltage implementation is appealing because generated voltages are directly compliant with the transistor supply in the selected 40 nm node, namely 1.1 V. However, low-voltage implementation is strongly impacted by channel length modulation and may require involved cascode circuits for correction thereby compromising available voltage ranges.

While channel length modulation might not be so relevant for long MOS channels, it becomes a key limitation for deep submicron technologies [12]. Indeed, gain limitation caused by finite output resistances is one major issue analog designers must confront for practical circuit design.

The impact of channel length modulation can be represented into first order by considering an equivalent Early voltage that is given as the inverse of λ parameter [4],

$$\boldsymbol{\lambda \propto \frac{\Delta L}{L}} \tag{18}$$

and assuming a linear variation of the pinch-off region length with V_{DS}, with *L* being the channel length. As CMOS technologies are scaled down, *L* decreases, thus increasing the parameter λ and decreasing the equivalent Early voltage. Hence, for similar current level, the output resistance decreases with *L* decreasing. This is of special relevance in the design of the low-voltage reference. In this circuit (see Figure 9), the operation principle is based in current mirroring through transistors M_1, M_2 and M_3. This mirroring is accurately obtained between M_1 and M_2, as their gates are shared, and their drains are connected to both inputs of a feedback amplifier. Hence, these drain voltages are virtually

equal due to the virtual ground effect, the error being inversely proportional to the amplifier gain. This error is not so relevant because is further attenuated by Early voltages and can, in any case, be controlled. Hence, we may assume that currents can be accurately copied.

This is not the case with transistor M_3. This transistor has its drain connected to a low impedance node, a resistance. And its voltage varies depending on the value of the resistance and the current used. Due to the higher dependence of current on V_{sd} voltage, an error in the copied current is introduced, with a small signal model the current is given by:

$$\boldsymbol{i_{mirror} = g_{m3} v_g + \frac{v_d}{r_{o3}}} \quad (19)$$

where the resistance r_o is inversely proportional to λ, modeling channel length modulation effect.

As temperature dependence of drain node voltage (V_{BE} voltage temperature dependence in the BJT for M_1 and M_2 drains) and channel length modulation (affecting M_3) differ from one another, a drift is introduced in the copied current, which is then induced in the voltage generated. A solution to this problem is introducing a boosted cascode mirror in M_3 as shown in Figure 10.

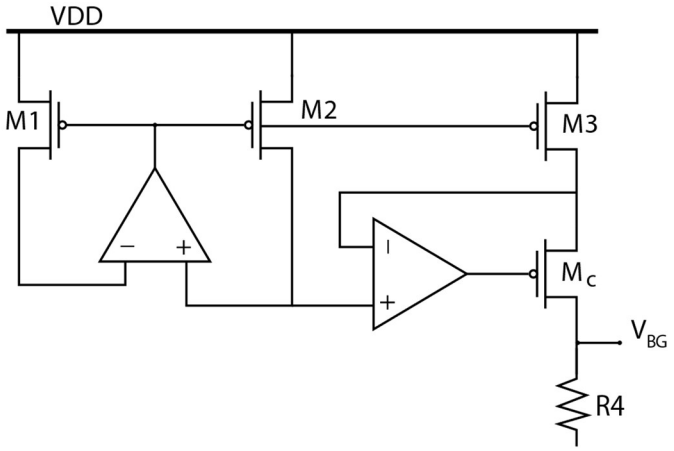


Figure 10. LOW-VOLTAGE BANDGAP SECTION WITH GAIN BOOSTED CASCODE

It is well known that the cascode transistor's function is to increase output resistance of the transistor, increasing this way its intrinsic gain too. With a boosted gain cascode, just by looking at the basic principles of the amplifiers function, we have that the voltage in the positive input is copied to the negative input, fixing M_3's drain voltage at the same value as M_2's.

A small signal analysis of the cascode stage highlights the contribution of this circuit regarding current mirror enhancement. Assuming the amplifier with a finite gain A and after applying basic circuit equations and some algebra we obtain the following expressions for the transconductance and the output resistance, respectively:

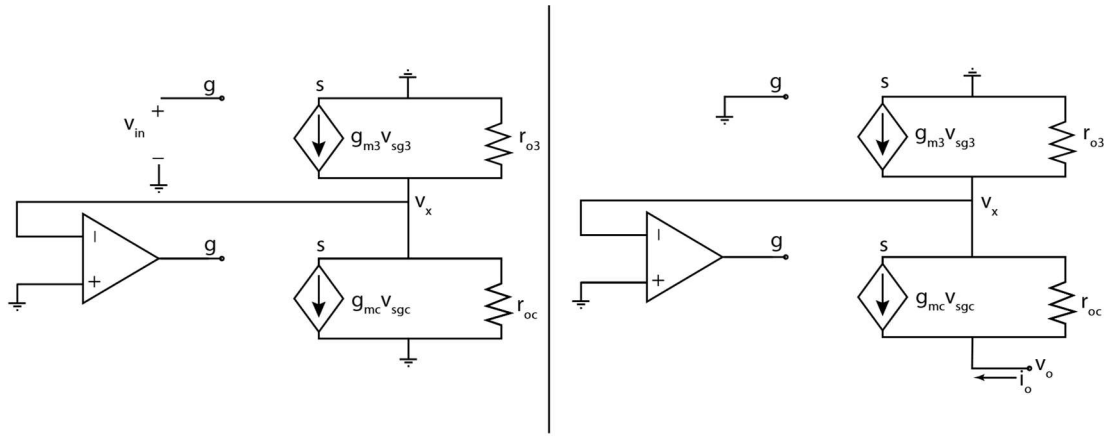


Figure 11. SMALL SIGNAL MODEL OF CASCODE STAGE, TRANSCONDUCTANCE CALCULATION (LEFT), OUTPUT IMPEDANCE CALCULATION (RIGHT)

$$G_M = \frac{i}{v_{in}} = g_{m3}\left(1 + \frac{r_{oc}}{r_{oc}r_{o3}g_{m3}(1+A) + r_{o3}}\right)^{-1} \approx g_{m3} \qquad (20)$$

$$R_{out} = \frac{v_o}{i_o} = r_{oc} + r_{o3} + (A+1)g_{m3}r_{o3}r_{oc} \approx (A+1)g_{m1}r_{o3}r_{oc} \qquad (21)$$

These two equations highlight that this stage acts like a transistor with transconductance G_M and output resistance R_{out}. This means, we can write the mirrored current by the small signal equation:

$$i_{mirror(casc)} = G_M v_g + \frac{v_d}{R_o} = g_{m3}v_g + \frac{v_d}{(A+1)g_{m1}r_{o3}r_{oc}} \approx g_{m3}v_g \qquad (22)$$

As opposed to what we saw in equation (19), the effect of drain voltage is reduced and almost neglectable, returning to the ideal behavior of the current mirror.

However, although using a boosted cascode circuit overcomes the channel length modulation problem, the cascode stage further reduces the already narrow voltage range available for the bandgap voltage. We are now left with a voltage range of $V = V_{DD} - 2V_{dsat}$, which in this technology was too low, particularly taking into account that the targeted application calls for reference voltages near to the supply rail. Hence, the standard voltage option was selected because the technology offers the possibility of using high voltage transistors.

2.1 ANALYSIS OF STANDARD VOLTAGE BANDGAP

Relevant design considerations for this architecture include stability, supply power rejection, and output noise.

2.2.1 STABILITY ANALYSIS

Although the bandgap circuit is meant to deliver DC voltages, it is a highly nonlinear structure that might exhibit several equilibrium states. For proper operation, the nominal equilibrium must be reachable and stable while other possible equilibria must be avoided. In other words, following switch-ON transient, the circuit must transverse a dynamic route leading it from zero voltage to the targeted output voltage and remain in equilibrium there. This is the so-called start-up transition.

This circuit has two stable states [4], namely:

- One spurious state where no current is flowing in either of the branches and voltage is zero in every point, which is a perfectly stable state from which the circuit won't exit unless forced to by an external influence.
- One nominal state that corresponds to the desired bandgap voltage generating state, where there's a current flowing through both branches and a voltage is generated.

A dedicated start-up circuit is needed to guarantee that the system reaches the nominal equilibrium state instead of the spurious one. The specific start-up circuit used in this design will be presented in Chapter 3. The next paragraphs address stability considerations about the nominal equilibrium point.

As we can see in Figure 8 the architecture has an amplifier with two feedback loops; one introduces positive feedback, while the other introduces negative feedback – see Figure 12. The negative feedback loop forces natural frequencies to move into the left half of the s-plane, while the positive feedback one drives natural frequencies to the right half. For stability, the composite natural frequencies must lie in the LHP.

Natural frequency locations can be assessed by writing the transfer function and analyzing the characteristic equation from

$$\boldsymbol{Y(s) = A(s)X(s) + A(\delta - \beta)Y(s) \rightarrow Y(s) = \frac{A(s)X(s)}{1 + (\beta - \delta)A(s)}} \qquad (23)$$

Stability can be assessed by either using Routh-Hurwitz´s criterion or resorting to Nyquist´s stability theory [13]. This latter option involves the loop gain $\boldsymbol{L(s) = (\beta - \delta)A(s)}$, and using the concepts of gain and margin phase. Specifically, the phase margin (PM) has to be positive [2]

$$\boldsymbol{PM = \angle\big((\beta - \delta)A(s)\big) - (-180°) > 0} \qquad (24)$$

This equation can be expressed as follows:

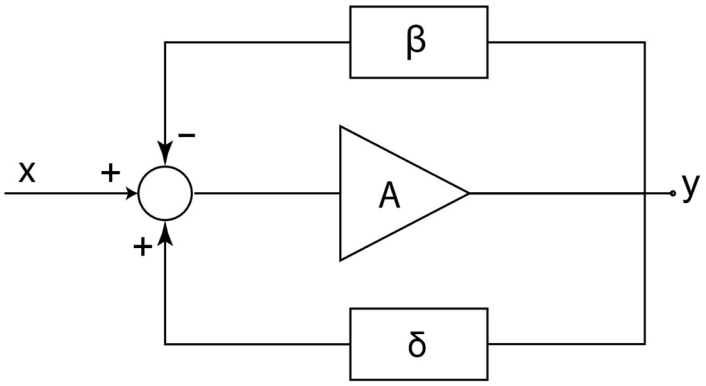


Figure 12. FEEDBACK LOOP BLOCK DIAGRAM

$$\angle \boldsymbol{L}(\boldsymbol{s}) = \angle\big((\boldsymbol{\beta}-\boldsymbol{\delta})\boldsymbol{A}(\boldsymbol{s})\big) = \angle(\boldsymbol{\beta}-\boldsymbol{\delta}) + \angle\boldsymbol{A}(\boldsymbol{s}) \tag{25}$$

Hence, if we ensure that the quantity $(\boldsymbol{\beta}-\boldsymbol{\delta})$ is positive, stability will only depend on the amplifier's phase margin in a buffer configuration where it's loop gain is given by:

$$\boldsymbol{L_{buffer}}(\boldsymbol{s}) = \mathbf{A}(\mathbf{s}) \tag{26}$$

It will hence suffice to guarantee that the amplifier is stable.

Of course, previous condition assumes that $(\boldsymbol{\beta}-\boldsymbol{\delta})$ is positive. Let us now calculate the values for these coefficients using a small signal model of the bandgap, so we can assess the transmittance of the feedback loops. Assuming the model of Figure 13 and after some algebra we obtain:

$$\boldsymbol{\beta} = -\boldsymbol{r_{d1}}\frac{\boldsymbol{g_{m1}r_{o1}}}{\boldsymbol{r_{o1}+R_2+r_{d1}}} \tag{27}$$

$$\boldsymbol{\delta} = -(\boldsymbol{R_1+r_{d2}})\frac{\boldsymbol{g_{m2}r_{o2}}}{\boldsymbol{r_{o2}+R_2+R_1+r_{d2}}} \tag{28}$$

To compare both transmittances and snice both transistors are biased with the same gate voltage and are symmetric, we have that $g_{m1} = g_{m2}$, and $r_{o1} = r_{o2}$. We can also derive r_d, which is obtained by linearizing BJT's characteristic in the operating point.

$$\boldsymbol{g_m} = \frac{\boldsymbol{\partial I_C}}{\boldsymbol{\partial V_{BE}}}\bigg|_{\boldsymbol{Q}} = \frac{\boldsymbol{I_C|_Q}}{\boldsymbol{U_T}} \rightarrow \boldsymbol{r_d} = \frac{\mathbf{1}}{\boldsymbol{g_m}} = \frac{\boldsymbol{U_T}}{\boldsymbol{I_C|_Q}} \tag{29}$$

To compare both transmittances and since both transistors are biased with the same gate voltage and are symmetric, we have that $g_{m1} = g_{m2}$, and $r_{o1} = r_{o2}$. We can also derive r_d, which is obtained by linearizing BJT's characteristic in the operating point:

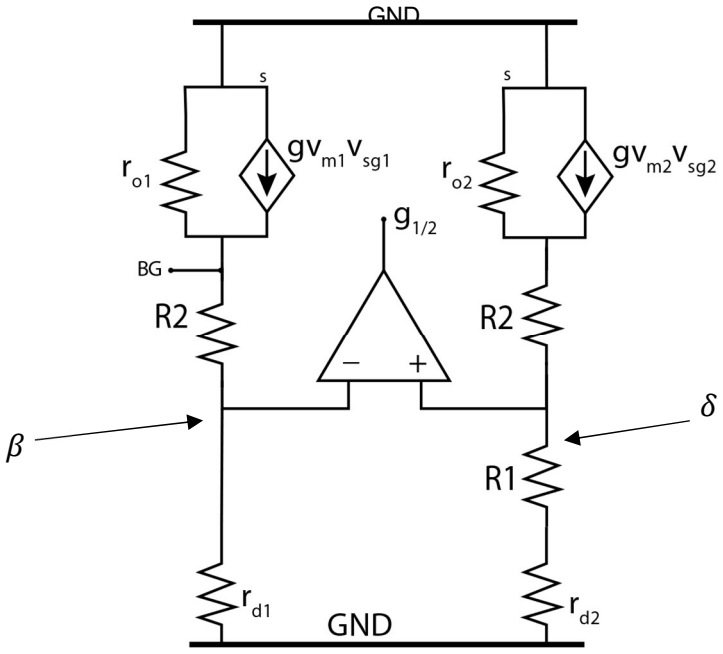


Figure 13. **SMALL SIGNAL MODEL OF THE BANDGAP REFERENCE**

$$\boldsymbol{g_m = \frac{\partial I_C}{\partial V_{BE}}\Big|_Q = \frac{I_C|_Q}{U_T} \rightarrow r_d = \frac{1}{g_m} = \frac{U_T}{I_C|_Q}} \tag{30}$$

There is also an "Early" resistance due to early effect, much larger than r_d but as they are in parallel, r_d dominates and r_o can be neglected, and a resistance associated to the term $r_\pi = (\partial I_B/\partial V_{BE})^{-1} = \beta_F r_d$, where β_F is the collector-base gain and is also in parallel with r_d so it's neglected. As we see form equation (30), r_d is only dependent on the base current, which is given by:

$$\boldsymbol{I_C = I_D(A)\left(e^{\frac{V_{BE}}{U_T}} - 1\right)} \tag{31}$$

Analysis of previous equations show that the dominant effect regarding r_{d1} and r_{d2} variations is the dependence of I_D with area. As the implementation of a BJT with *N* times the area is equivalent to *N* parallel transistors, in the small signal analysis, it will behave as *N* parallel resistances. As current in both branches is the same, we have that $r_{d1} = r_d$ and $r_{d2} = r_d/N$, thus yielding:

$$\boldsymbol{(R_1 + r_d/N)\frac{r_o}{r_o + R_2 + R_1 + r_d/N} - r_d\frac{r_o}{r_o + R_2 + r_d} > 0} \tag{32}$$

This expression verifies the stability of the bandgap for the symmetric case. The value of r_d, being the resistance of a diode, can be neglected.

2.2.2 POWER SUPPLY REJECTION (PSR)

Power supply rejection is an important parameter in these circuits as reference voltages must maintain their value with variations in the supply voltage that can be caused by the noise of different types including RI drops, crosstalk, dI/dt drops, and switching noise [14] among others.

The circuit we are confronting for this analysis is a complex one, that can increase the confusion during calculations. To make power supply analysis possible, we will follow the strategy proposed in [15]. We will envision the system as a two-stage amplifier circuit for this task. The first amplifier is clear as it is the amplifier in the circuit, but this time we will represent both the transistors as amplifiers too. In a small signal analysis for PSR, we are supplying the input through the source of the transistor, with a fixed gate voltage. This configuration of the transistor as an amplifier is known as the common gate amplifier. But we will also have the gate voltage vary through the effects of the supply variations in the amplifier's output, it would be as having the device in Figure 14.

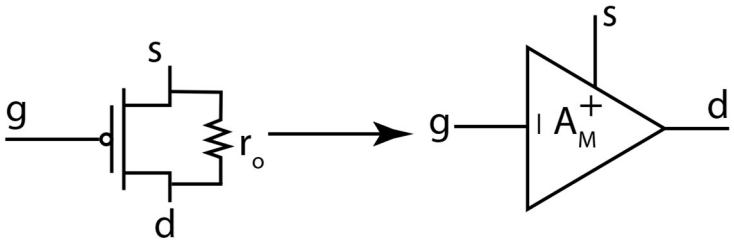


Figure 14. AMPLIFIER VISUALIZATION OF CMOS

Both inputs in Figure 14 have a small signal gain $A_M = g_m r_o$, with a sign indicated by the input in the symbol. This is not a differential amplifier and must just be seen as a symbol that eases the next analysis done. We can turn the schematic of the bandgap now into the small signal model with input in the supply voltage seen in Figure 15.

From here we can obtain the different contributions to the PSR. In the diagram we have the amplification of both transistors through both their input terminals (s and g) and because their biasing is the same, they are assumed in the same operating point and with the same gain, this way we can represent both with only one amplifier that opens into two feedback loops. We also have the amplifier's differential gain, and a supply to output gain for the amplifier alone ($A_{p1} = V_x/V_{DD}$), which is the PSR of the amplifier. With this we can obtain the PSR for the bandgap with the following expression:

$$\boldsymbol{v_{out} = A_{p2} v_{dd} - A_{p1} A_2 v_{dd} - A_M A_1 \left(\frac{R_1 + \frac{r_d}{N}}{R_1 + R_2 + \frac{r_d}{N}} - \frac{r_d}{R_2 + r_d} \right) v_{out}} \quad (33)$$

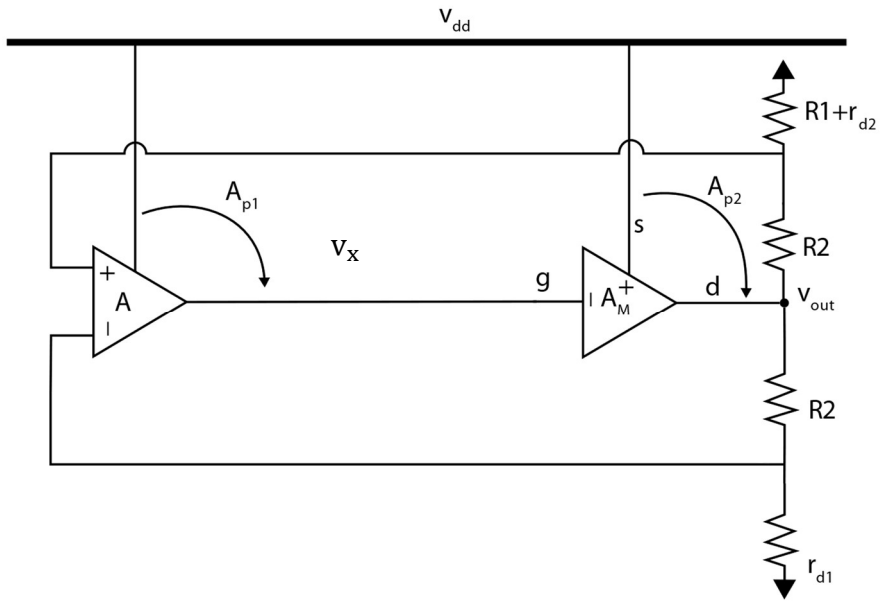


Figure 15. SCHEMATIC FOR PSR ANALYSIS

Reordering the terms, we obtain:

$$\boldsymbol{PSR = \frac{v_{out}}{v_{dd}} = \frac{A_{p2} - A_{p1}A_2}{1 + A_M A_1 \left(\frac{R_1 + \frac{r_d}{N}}{R_1 + R_2 + \frac{r_d}{N}} - \frac{r_d}{R_2 + r_d} \right)} v_{dd}} \quad (34)$$

Several conclusions can be made from the previous equation:

- The first is the critical importance of a good amplifier design in the final performance of the overall system of the voltage reference. We can see two dependences in equation (34), the higher the gain of the amplifier, the better the supply rejection, this is a direct consequence of the differential implementation. As the bandgap is symmetric, difference between V_+ and V_- are caused by offset, that are a consequence of finite gain in the amplifier, hence the higher the gain, the lower the error. We also need to notice that gain is a function of frequency $A = A(s)$ and as frequency increases, the gain decreases, deteriorating supply rejection for higher frequency noises.
- As the amplifier is directly powered from the supply rails, its own power supply rejection will have an influence in the total bandgap's *PSR* as we see in the factor A_{p1}, the lower the gain from supply to the amplifier output, the better the bandgaps *PSR*. Finally, we have the effect of transistor common gate amplifier configuration with respect to supply in this aspect, we also need to decrease the gain, as it depends on g_m so we would need a design with low g_m for mirroring transistors.

2.2.3 NOISE SOURCES IN THE VOLTAGE REFERENCE

Noise calculations involve identifying the noise sources and their transfer functions to the output voltage node V_{bg}. The main noise sources are represented in red in Figure 16.

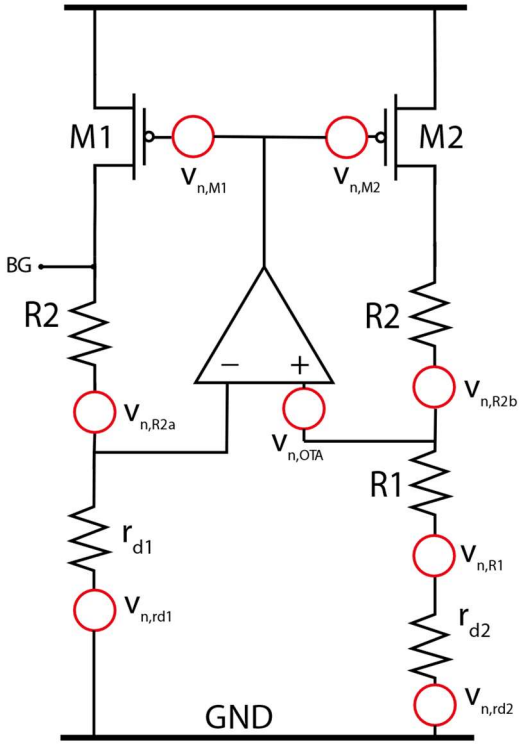


Figure 16. NOISE SOURCES IN BANDGAP

The output referred noise for the system considering all the noise inputs, can be calculated as [16]:

$$\boldsymbol{RMS_n^2 = \sum_i \overline{v_{n,i}^2} \cdot |H_i|^2} \tag{35}$$

where $\overline{v_i^2}$ are the noise densities at the input of the devices, while $|H_i|$ their transfer functions from the input of the component to the output of the bandgap v_{bg}.

We will first give the values for the input noise densities of different components. These are well-known values derived from statistical and thermodynamic principles and can be found in many circuit design books as [2] and [4]. The values are given in the expressions below.

$$\boldsymbol{\overline{v_{n,R}^2} = 4k_BTR} \tag{36}$$

$$\boldsymbol{\overline{v_{n,M}^2} = \frac{4k_BT}{g_m} + \frac{K}{C_{ox}WL \cdot f}} \tag{37}$$

$$\overline{v_{n,OTA}^2} = 8k_BT\left(\frac{1}{g_{m,dp}} + \frac{g_{m,mirr}}{g_{m,dp}^2}\right) \quad (38)$$

These equations account for the thermal noise of the three main components, and the flicker noise of the MOS transistors. Here $g_{m,dp}$ is the differential pair transconductance in the amplifier and $g_{m,mirr}$ the transconductance in the current mirror, constant *K* is technology dependent. We are left with the calculation of the different transfer functions.

Table 1 shows two behaviors for both branches, we have for the output branch a direct transfer function that only depends on the branch, while for the second branch we have it multiplied by the amplifiers transfer function $|H_{OTA}|$. This means that all the noise from the second branch will be filtered by the amplifiers transfer function.

Table 1. NOISE TRANSFER FUNCTIONS

Component	Transfer function	Component	Transfer function
$\|H_{M1}\|^2$	$g_{m,M1}^2 \cdot \left(r_o \| \| (R_2 + r_d)\right)^2$	$\|H_{M2}\|^2$	$g_{m,M2}^2 \cdot \left(r_o \| \| (R_2 + r_d + R_1)\right)^2 \cdot \|H_{OTA}\|^2$
$\|H_{R2a}\|^2$	$\left(\frac{r_o}{R_2 + r_d + r_o}\right)^2$	$\|H_{R2b}\|^2$	$\left(\frac{\mathrm{r_o}}{R_2 + \mathrm{R_1} + r_d + r_o}\right)^2 \cdot \|H_{OTA}\|^2$
$\|H_{r_{d1}}\|^2$	$\left(\frac{r_o}{R_2 + r_d + r_o}\right)^2$	$\|H_{rd2}\|^2$	$\left(\frac{r_o}{R_2 + \mathrm{R_1} + r_d/\mathrm{N} + r_o}\right)^2 \cdot \|H_{OTA}\|^2$
$\|H_{OTA}\|^2$	$A^2 g_{m,M1}^2 \cdot \left(r_o \| \| (R_2 + r_d)\right)^2$	$\|H_{R1}\|^2$	$\left(\frac{r_o}{R_2 + \mathrm{R_1} + r_d/\mathrm{N} + r_o}\right)^2 \cdot \|H_{OTA}\|^2$

From these results, we can extract some interesting trends for the design process. As we observe we can control the noise from transistors and amplifier through careful design, which are the main noise sources in the bandgap [1], we will see how to take advantage of these expressions.

Regarding the transistor's noise, the output referred noise coming from this source can be expressed as follows:

$$RMS_{n,M1}^2 = \left(r_o \| \| (R_2 + r_d)\right)^2 \cdot \left(4\mathrm{k_B}T\mathrm{g_{m,M1}} + \frac{K \cdot \mathrm{g_{m,M1}^2}}{C_{ox}WL \cdot f}\right) \quad (39)$$

First, we focus on the flicker noise, the second contribution to the noise in equation (37). As we see, this noise is dominant for lower frequencies as it is inversely proportional to f, as well as to the rea of the transistor, which we can see in the factor WL. We see that bigger transistors have lower flicker noise.

On the other hand, we see in both terms in equation (39) direct dependance with transistor's transconductance g_m, this parameter is given by the following expression:

$$\boldsymbol{g_m = \mu_o C_{ox} \frac{W}{L} V_{dsat}} \quad (40)$$

As we can see, a lower g_m benefits the output noise of the bandgap for both transistors M_1 and M_2. We also recall from equation (34), that PSR improves with a low gain from v_{dd} to v_{bg} through transistors, which implies a low g_m will improve *PSR* and noise features of the bandgap at the same time.

We also have to consider the amplifier's effect on noise. As we see in Table 1, amplifier's noise will also be affected by the transistor $M1$ transfer function, so the same principles will still apply. Apart from this, we have the gain factor of the amplifier A. It is obvious from the expression that a lower gain will imply lower noise, but this election has serious tradeoffs. Lower gain implies an increase in non-ideality effects [17], lower bandgap precision, higher variability with process variations [18], and a worse PSR parameter, as we saw in the previous analysis. Careful consideration has to be taken for this design decision.

Gain not only affects with its DC value, but we have to also acknowledge its frequency dependence, as noise is not a DC property. Noise will be highly dependent on amplifiers bandwidth. The lower bandwidth, the less noise can get to the output, as amplifier stops acting as so for higher frequencies and noise cannot pass. With a higher bandwidth, a higher noise bandwidth will get to the output. We still have to ponder bandwidths effect on *PSR*, as a lower bandwidth will deteriorate *PSR* for higher frequencies, as we see in equation (34).

Finally, by using equation (38) we observe that for a low noise amplifier we must design it with a low value of g_m for the current mirrors in the amplifiers, this is because they act as current sources and the value of the small signal current varies following the relation $i = g_m v_g$, so a low g_m will be less sensible to small variations in v_g.

CHAPTER 3- CIRCUIT DESIGN: SCHEMATIC AND LAYOUT

Based on the analysis in previous chapters, the design proceeds covering several steps:

i. The value of *N* is selected based on BJT scaling considerations.
ii. The current flowing through each branch is selected thus setting the value of R_1.
iii. Using these previous values, temperature dependence measurements determine the value of R_2.
iv. Once currents are set, W/L transistor ratios are selected according to the current and the targeted operation regions.
v. The amplifier is designed to cope with the gain and low-noise requirements described in the previous chapter.

Details on the bandgap design require technology parameters such as:

- β in the current equation of the transistor,
- mobility of holes and electrons,
- variation of g_m with biasing and size, etc.

Numerical values for these parameters cannot be published in this thesis as they are under an NDA agreement. Hence, this document provides a general view of the design process and a summary overview of the validation results.

3.1 PARAMETER SCALING OF BANDGAP CORE

3.1.1 RESISTANCE SCALING

The first decision is current. In this design, current was chosen to be of $70\mu A$ per branch. It is a high current, but it implies larger transistors which reduce flicker noise, as well as reduced values for resistances decreasing thermal noise from them according to equation (36). We also decide the area ratio between BJT transistors, which will determine the voltage difference between V_{BE} and V_{BE2}. To ease the layout design, we select a ratio $N = 8$, which allows us to easily implement a common centroid layout design of BJT transistors that enhances matching [19], as we will see in the layout design section.

Given the branch current and the BJT area ratio, the R_1 value is calculated from equation (12), yielding:

$$\boldsymbol{R_1 = \frac{U_T log(N)}{I} = 770\Omega} \qquad (41)$$

Concerning the resistance R_2 , calculating its value involves a semi-empirical approach that requires simulations. The procedure relies on equation (13). This equation gives us the value of V_{bg}, but we need it to be temperature independent, so we differentiate the relation.

$$\boldsymbol{\frac{\partial V_{bg}}{\partial T} = \frac{\partial V_{BE1}}{\partial T} - \frac{\partial \Delta V_{BE}}{\partial T} = \frac{V - (3+m)U_T - \frac{E_g}{k}}{T} + \frac{R_2}{R_1} \cdot \frac{k_B}{q} = 0} \qquad (42)$$

As already mentioned in Chapter 1, this equation highlights that we cannot cancel out temperature dependence in the whole range because curvatures are different. We must decide to center the design at a temperature where the temperature coefficient will be 0. For this design, it was decided to center the bandgap reference design at room temperature ($297\ K$), which means, equation (42) must be satisfied at the desired temperature. As we can observe, V_{BE} temperature dependance is complex and includes technology dependent parameters, so evaluation of the ratio R_2/R_1 must be done through simulation using Cadence software (see Figure 17).

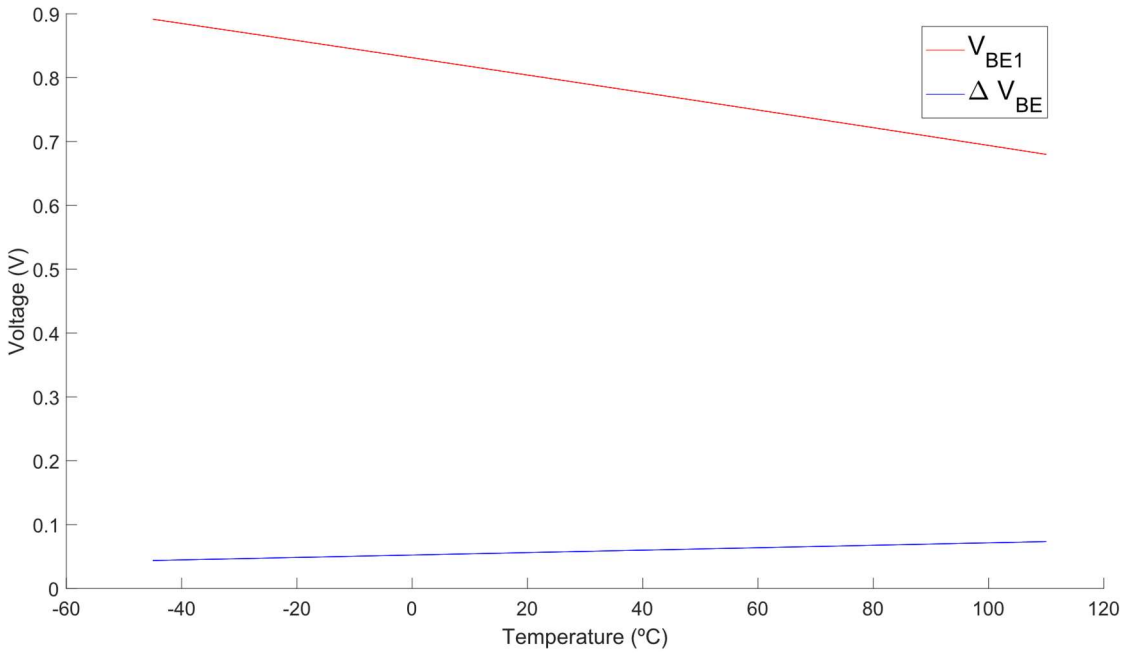


Figure 17. PTAT-CTAT VOLTAGES AGAINST TEMPERATURE

From this evaluation we find that $R_2/R_1 \approx 8$. From where we obtain a first estimation of R_2. After this we will have to sweep around the values obtained for both resistances so that we obtain cancellation at the precise point we want it.

3.1.2 g_m/i_d METHODOLOGY FOR M_1 AND M_2 SIZING

For the outmost part of the bandgap, we are left with the sizing of transistors M_1 and M_2 (see Figure 8). As highlighted in equation (39), the g_m of these transistors is subjected to trade-offs involving the thermal noise, on the one hand, and flicker noise, on the other hand. To find the correct values of W and L we will use what's known as g_m/i_d methodology for scaling.

The g_m/I_D methodology as its name suggests uses the transconductance efficiency (g_m/I_D) as main parameter to determine MOST size W/L. This parameter's usefulness comes from the universality property of transconductance efficiency, this means, it is largely independent of MOST process except for the substrate factor n, which depends on the relation between gate capacitance and source depletion region capacitance (C_{js}) as shown below:

$$\boldsymbol{n = 1 + \frac{C_{js}}{C_{ox}}} \tag{43}$$

n has a value between 1.3 and 1.5 typically [20].

For CMOS technologies, transconductance efficiency varies continuously from 25-30 in weak inversion (the most gain-efficient region) to 2-5 in strong inversion.

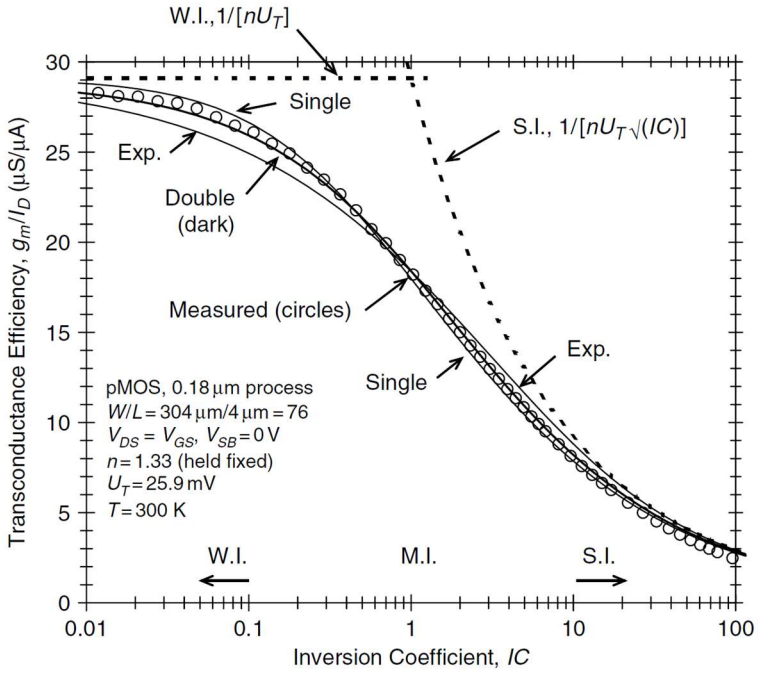


Figure 18. g_m/I_D **TYPICAL FIGURE, PREDICTED AND MEASURED VALUES [20]**

With g_m/I_D we exploit the fact that this ratio does not depend on [21]. Following this idea, we can determine the needed *L* for the desired g_m value, which is determining the inversion region in which we will be working. Once the

L that achieves the g_m/I_D parameter desired is found, we can scale the *W* to the one required to obtain the desired drain current with the proportionality relation in equation (44).

$$\mathbf{W'} = \boldsymbol{W}\frac{\boldsymbol{I_D'}}{\boldsymbol{I_D}} \tag{44}$$

where W' and I_D' are the target values and W and I_D are the values used while obtaining the g_m/I_D curve (while obtaining this curve W can be selected arbitrarily as it does not affect and I_D will scale accordingly).

We illustrate the procedure through the sizing of transistors $M_1$and M_2. We found in last section that in order to diminish as much as possible noise, we needed a low g_m value. We select for this a low transconductance efficiency, which means we will get transistors into strong inversion region with a $g_m/I_D \approx 5-6$, as it is also inversely proportional to V_{dsat} and we need to ensure that there's range for everything to work correctly. Once obtained the L of $0.32\ \mu m$, we obtain W needed for the selected I_D. We then scale it up to increase the area WL to reduce flicker noise. We then have $W/L = 7.68$. With this we have the bandgap core scaled. We need to make fine adjustments to the parameters such as resistances and transistor sizes through simulation so that they account for temperature dependence of elements with lower impact such as the resistances. As we still haven't designed the amplifier we use for this purpose a model, that will help us determine DC gain and BW for the amplifier. The model used is a voltage-controlled current source connected to an RC circuit.

3.2 AMPLIFIER DESIGN

In this section we will review the general design of a two-stage transconductance amplifier. For this design, a 5-transistor first stage was chosen. For the second stage, a common source amplifier is enough, we can see the architecture chosen in Figure 19.

To start the design procedure, we need to mark the objectives, which in this case can be summarized in the gain and the frequency response

- Regarding the gain, the target is 1000, or 60 dB. This minimizes the virtual ground error to around 0.1%, as it is inversely proportional to gain. This ensures correct operation of the bandgap as it fixes the same voltage for both R_2 resistances, thus also ensuring the same V_{ds} minimizing channel effect errors in the current biasing of the branches.
- Regarding frequency response, we need a wide enough bandwidth that ensures supply rejection for a wide range of frequencies, as we saw in section 2.2.2. As a design parameter, better than bandwidth is *GBW*, which is independent of the feedback loop, unlike bandwidth [4]. We set this to a value of at least 10 MHz.

Once parameters are set, we can begin our design task. Bias current introduced through M_b is obtained from the bandgap core, mirroring the branch currents, and is reduced to $20\ \mu A$ to reduce power consumption.

Regarding design equations for this amplifier. It is commonly known that the first stage gain can be obtained as [2]:

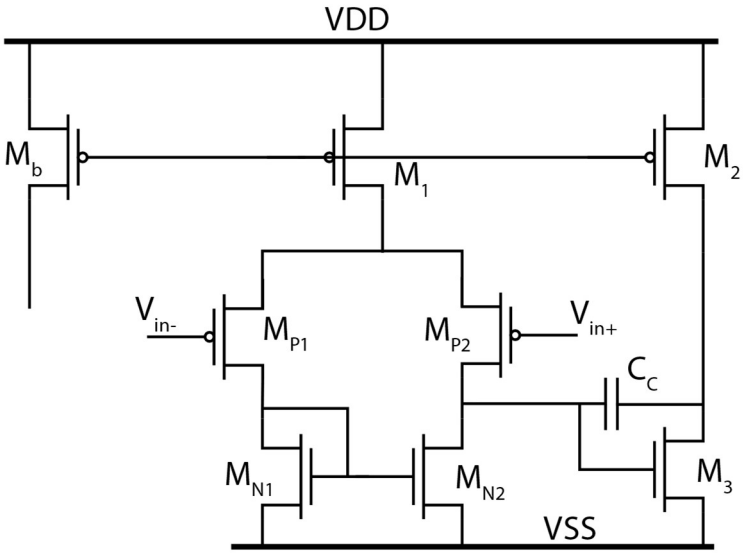


Figure 19. TWO-STAGE OTA ARCHITECTURE

$$\boldsymbol{A_1 = g_{mN} \cdot (r_{op2} || r_{on2})} \tag{45}$$

and the second stage as:

$$\boldsymbol{A_2 = g_{m3}(r_{o3} || r_{o2})} \tag{46}$$

The gain bandwidth (*GBW*) is expressed as:

$$\boldsymbol{GBW = \frac{g_{m1}}{C_c}} \tag{47}$$

GBW is determined by this expression because we use a Miller capacitance to compensate and stabilize the amplifier, making the 1st pole of the amplifier much lower than the second, separating them by applying Miller's theorem. With this, we obtain a phase margin of 60º which ensures stable operation of the amplifier. To locate the second pole of the transfer function of the amplifier, we evaluate the load capacitance, which in this case is the sum of the two gate capacitances of the bandgap transistor, in the order of $25\ fF$.

These expressions can be deduced from a simple small signal analysis. As we have two stages, we should divide the gain in the two stages, so it is more feasible, and we can set the objectives of each transistor. We set as reasonable

values for each one, a gain of 40 dB for the first stage and a 20 dB gain for the second.

Next, we have to set the geometry of the transistors, as we know from the noise analysis of the previous chapter and equation (38) specifically, an amplifier needs a high transconductance in the differential pair in this case, PMOS, and a low transconductance in the current mirror, NMOS. The methodology to size transistors this time is based directly on equations modelling the transistor. As we know transconductance is given by:

$$\boldsymbol{g_m = \frac{\partial I_D}{\partial V_{gs}} = \frac{2I_D}{V_{dsat}}} \tag{48}$$

As we have 3 transistors stacked, we need to ensure we can fit 3 V_{dsat}, which in this case is not a very restrictive demand. We aim for a g_m of $100\ \mu A/V$ and an output resistance of $1M\Omega$ to obtain the desired 40dB of gain. For the NMOS transistor we aim for a $40\ \mu A/V$, following noise reduction rules. For this we measure the effective β_{eff} parameter ($\approx \mu C_{ox} W/L$) and using the known value of $I_D = 10\ \mu A$ (half bias current for each branch), we can obtain the V_{dsat} value and from there apply equation below.

$$\boldsymbol{I_D = \mu C_{ox} \frac{W}{L} (V_{dsat})^2} \tag{49}$$

To obtain the needed W/L scale for each 1st stage transistor. Which results in the following scaling.

Table 2. 1ST STAGE AMPLIFIER TRANSISTOR SIZING

Transistor	W	L
PMOS	$6\ \mu m$	$0.6\ \mu m$
NMOS	$1.2\ \mu m$	$1.6\ \mu m$
MB	$0.6\ \mu m$	$0.4\ \mu m$
M1	$1.2\ \mu m$	$0.4\ \mu m$
M2	$0.6\ \mu m$	$0.4\ \mu m$

Next, we need to size the transistor for the 2nd stage. Here, the NMOS transistor that constitutes the amplifier is fully dependent on the size of the first-stage amplifier, as we will justify in the next lines.

As we know, current driven by a transistor in saturation region is given by equation (49) without channel effect. In the case of transistors M_{N2} and M_3 this V_{dsat} is $V_G - V_{SS}$. M_{N2} is part of a current mirror in which M_1's gate is shorted with its drain, making $V_{gs\,N1} = 0$. In equilibrium (which is the most common large signal

state for this circuit with a common mode voltage at both inputs) M_{N1} and M_{N2} drive a current $I_{bias}/2$, and their V_d is ideally the same, making $V_{dN2} \approx V_{gN2}$ as $V_{dN1} = V_{gN1}$. M_{N2}'s drain is shorted with M_3's gate, making $V_{d3} = V_{gN2}$,thus $V_{gs3} = V_{gsN1} = V_{gsN2}$, this means they have the same V_{dsat}, and current driven by M_3 follows the relation:

$$\frac{\mathbf{I_{M3}}}{\boldsymbol{I_{MN2}}} = \frac{(\boldsymbol{W/L})_{\boldsymbol{M3}}}{(\boldsymbol{W/L})_{\boldsymbol{MN2}}} \tag{50}$$

The size of M_3 must be scaled according to the current ratio between both transistors to guarantee that its gate voltage is equal to that of M_{N1} and M_{N2}. Taking this into account, we doubled the current of the second stage, to enhance gain, thus the size of M_3 is determined by:

$$\left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\boldsymbol{M3}} = \mathbf{4}\left(\frac{\boldsymbol{W}}{\boldsymbol{L}}\right)_{\boldsymbol{MN2}} \tag{51}$$

Table 3. 2ND STAGE TRANSISTOR SIZING

Transistor	W	L
M3	$1.2\ \mu m$	$1.6\ \mu m$

We finish by adding Miller´s compensation to the amplifier, so that the phase margin is positive, and the overall system is stable as long as we ensure feedback is negative as we saw in 2.2.1.

Compensation is the main goal of capacitance C_C, which makes use of Miller's theorem which states that the two circuits in Figure 20 are equivalent with the values of Y_1 and Y_2 given by [2]:

$$\boldsymbol{Y_1 = Y(1 + A)}; \qquad \boldsymbol{Y_2 = Y\left(1 + \frac{1}{A}\right)} \tag{52}$$

In our case $Y = C_C$.

We want our systems to have a GBW defined by the first pole of the system, separating the second pole so that the system is stable. As GBW is set by $GBW = A_o p_1$ we want $p_2 > A_o p_1$. Poles in the system are given by:

$$\boldsymbol{p_1 = \frac{1}{r_{o1} C_{L1}}}; \quad \mathbf{p_2 = \frac{1}{r_{o2} C_{L2}}} \tag{53}$$

Using these equations and taking into account a $10MHz$ *GBW* goal set in the beginning, we obtain the parameter for the design, with $C_c = 67\ fF$.After some fine adjustments using the qualitative guidance of previous design equations we obtain the design parameters in Table 4.

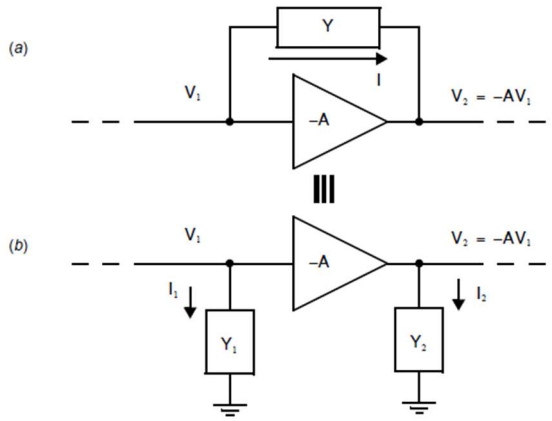


Figure 20. MILLER'S THEOREM REPRESENTATION [2]

Table 4. AMPLIFIER DESIGN PARAMETERS

$(W/L)_{MB}$	1.5
$(W/L)_{M1}$	3
$(W/L)_{M2}$	6
$(W/L)_N$	10
$(W/L)_P$	0.75
$(W/L)_{M3}$	3
C_c	$67\ fF$
r_{out1}	$1\ M\Omega$
g_{m1}	$80.9\ \mu A/V$
A_1	$38\ dB$
r_{out2}	$205.7\ k\Omega$
g_{m2}	$251.1\ \mu A/V$
2	$34\ dB$
GBW	$50\ MHz$

3.3 START-UP CIRCUIT

As discussed in Section 2.2.1, the bandgap circuit has two stable states, namely:

- a current-flowing state that generates the desired voltage, and
- a no-current state, also stable that doesn't generate any voltage at all. In this state amplifier's output voltage node is at a high level, leaving both transistors' channels OFF so that there is no current in either branch.

As the latter is a stable state, the system won't leave it unless forced to, which is the main goal of a start-up circuit, forcing the system out of the no-response state.

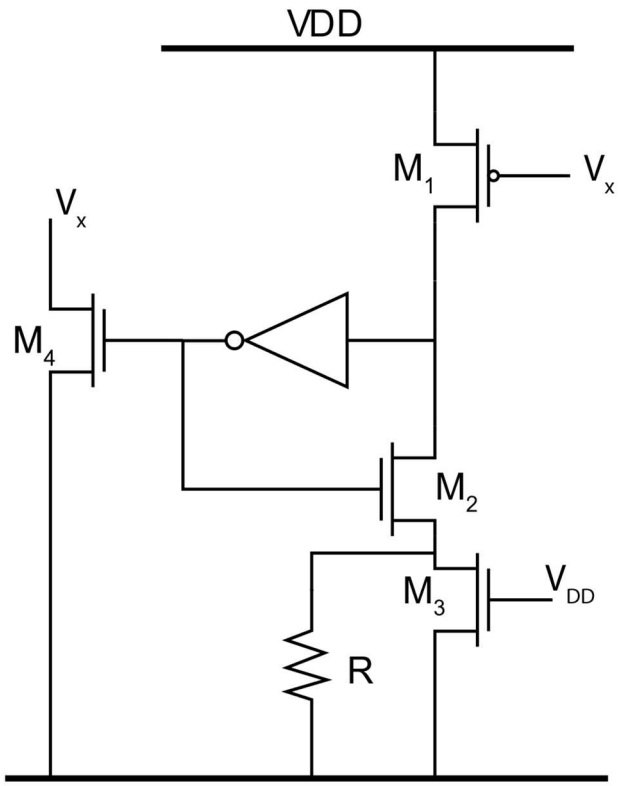


Figure 21. **START-UP CIRCUIT SCHEMATIC**

Figure 21 shows the schematics of the circuit employed for start-up. In this circuit, V_x is the output node of the amplifier, whose voltage has to be pulled down to drive transistors' channels ON. The working principle is as follows. If V_x is at a high voltage level, M_1 transistor is closed, isolating inverter input from V_{DD}, which is then at a lower level, this makes it output get to a high level that triggers M_2 and M_4, which now have their channels open. M_4 connects V_X to ground, pulling the voltage down and opening bandgap transistors, while M_2 keeps inverter input low while start-up is working. Once V_x voltage is low enough, M_1 starts driving current, pulling inverter's input to a higher voltage and closing gradually M_4 and M_2. Once the voltage V_x reaches its correct level, the start-up circuit reaches an equilibrium, cutting its influence on the node voltage.

The main design preoccupation in this circuit is to ensure that M_1 can drive enough current to pull the inverter's input node voltage up, opposing the action of M_2. All transistors are kept at minimum size except for M_1 with 3 times the minimum width to ensure current driving power.

3.4 LAYOUT DESIGN

Once the whole schematic level design is completed and checked by simulation (see Chapter 4 for validation results), we are left with the layout design. This step allows us to extract parasitics that can affect the behavior of the circuit and

simulate their effects. We can also check our physical design fulfills all design rules and corresponds with the schematic design through DRC (Design Rule Check) and LVS (Layout vs Schematic) tests.

A key point to be considered during the layout phase concerns matching techniques. We have to ensure minimal variations of the circuit through our design. Particularly, besides short correlation distance variations that are dependent on devices´ areas and shapes [19], gradients and linear errors can be partially accounted for by using common-centroid layout techniques [22].

All in all, the final goal is that actual ratios between large-signal transistor transconductance parameters keep the closest possible to the nominal values. Consider for instance the ratio between M_{N2} and M_3 which nominal value is 4 to ensure correct drain voltage in transistor M_{N2} and avoid current mirror error (see Section 3.2)3.2. Figure 22 shows the corresponding layout using common-centroid style. It can be seen that common centroid is achieved in each component of the amplifier, it is especially visible in the 1st stage mirror and 2nd stage, which correspond to M_{N1}, M_{N2} and M_3 transistors. In the center box we see transistors M_{N1} and M_{N2} symmetrically placed with the symmetry axis place approximately in the green metal line. M_3 transistors correspond to the 4 other structures connected in parallel forming a transistor 4 times larger than M_{N1} and M_{N2} as we wanted, with a symmetry center at the center of the structure. The rest of the structure follows a similar design structure.

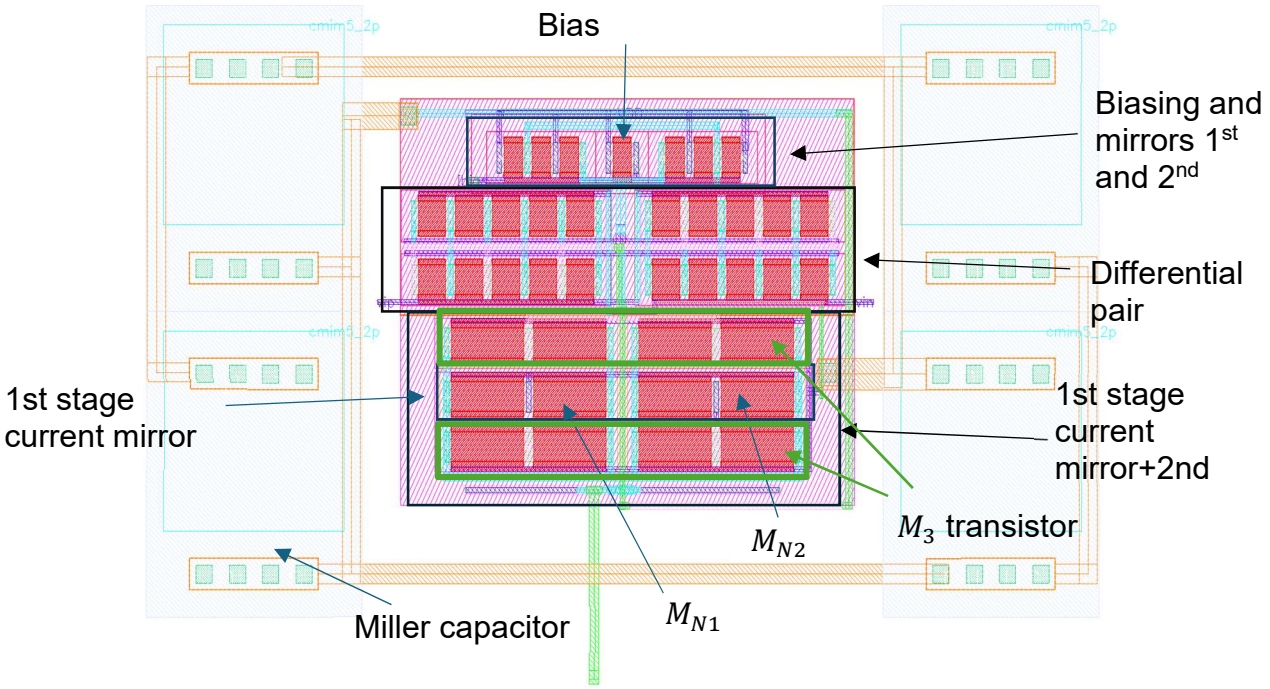


Figure 22. **TWO-STAGE AMPLIFIER LAYOUT DESIGN**

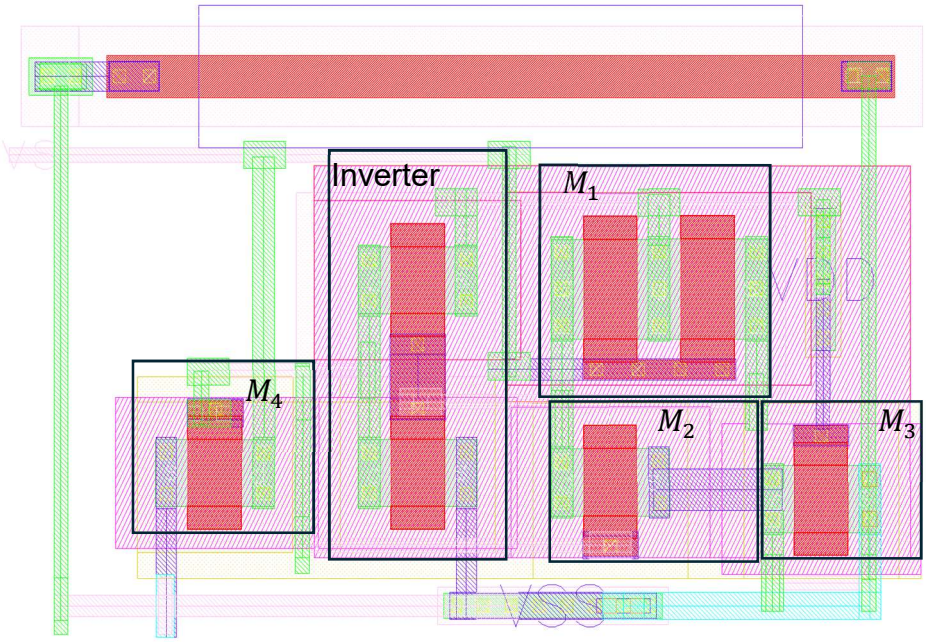


Figure 23. START-UP LAYOUT DESIGN

Consider now the start-up layout. In this circuit, matching is not as important as its main function is pulling node voltage down and precision is not needed. The main goal in the layout of this section is area optimization. Figure 23 shows its layout where the only constraint is to keep transistor separations within the margins imposed by the foundry design kit.

Figure 24. shows the complete bandgap circuit layout, composed of the amplifier circuit and the start-up. We see the different parts, such as the amplifier, the start-up circuit, etc. The transistors M_1 and M_2 are implemented with a common centroid in a similar way as the previous design to match branch currents as well as they can. In the top right corner, we see the BJT transistors that occupy most of the area. As we said in the previous chapter, relation N=8 was selected for a common centroid design. The center square is transistor Q_1 while the network of 8 squares surrounding it implements transistor Q_2 with 8 times the area we need for the bandgap implementation.

Regarding resistors, several options are available in this technology. We have siliceded and unsiliceded, poly and OD resistors. And in each of them, we have N and P versions of them. After a revision of documentation, we can check that P+ unsiliceded poly resistors present the lowest temperature variation of all, with a parabolic dependency. It also presents the most area-efficient option.

Total area is $31\ \mu m \times 36\ \mu m$.

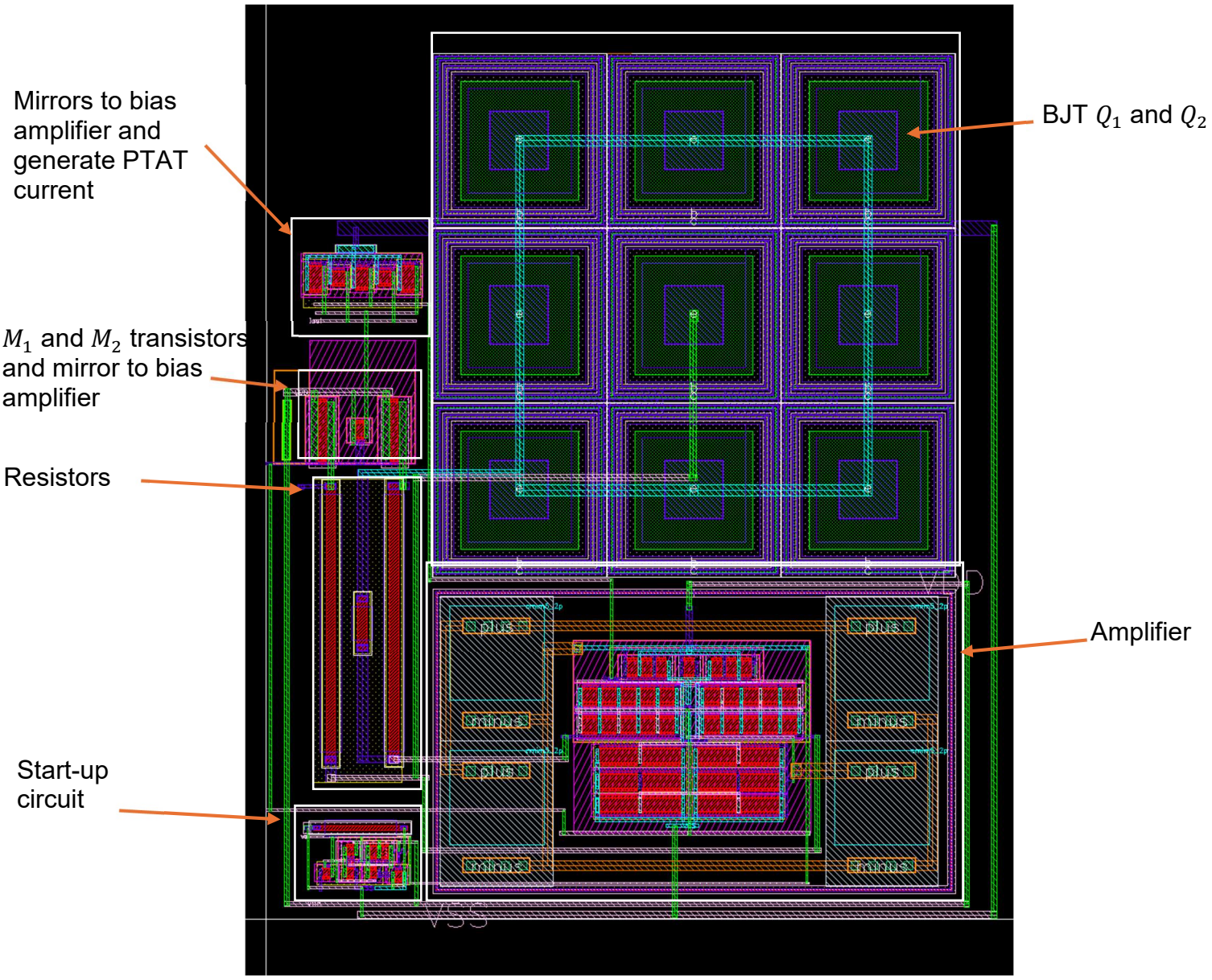


Figure 24. BANDGAP LAYOUT

CHAPTER 4- TESTS AND RESULTS ANALYSIS

To conclude the design, we have to test the circuit to check that it works correctly, and design goals are achieved with the parameters obtained in Chapter 3. Simulations were run during the process of design at various points of the process. Schematic-level simulations of amplifier were done before incorporating it into the system, and schematic-level simulations of the system were done before the process variation test, but to obtain a clear structure in this thesis, all simulations are shown in this final chapter.

4.1 AMPLIFIER SIMULATIONS

We begin by examining the results of the amplifier. As we established in the previous chapter, the amplifier's goals were a DC gain greater than 60dB, a GBW of 1MHz, and a stable operation in any configuration possible.

To check these design objectives are fulfilled we use the following test structure. The amplifier will be connected in a buffer configuration, this way we test the worst possible case of feedback. If we remember from section 2.2.1, by ensuring the phase margin in this configuration is positive, we can be confident that with any negative feedback the amplifier will still have a stable operation. On the other hand, we know GBW is independent of the feedback loop applied [2]. We can see the buffer configuration in Figure 25.

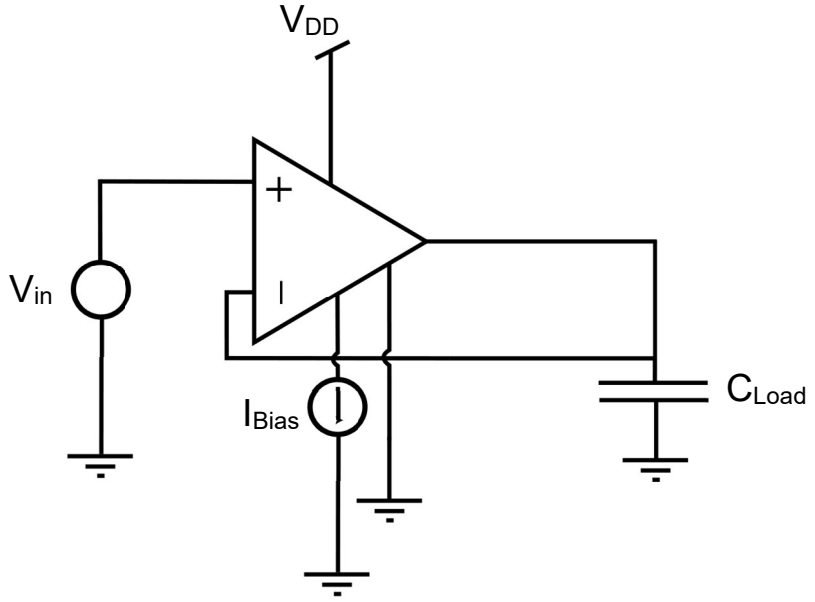


Figure 25. BUFFER CONFIGURATION FOR TEST

To simultaneously test all three parameters we will run a stability simulation by introducing an AC excitation with variable frequency and an amplitude of 1 V through V_{in}. This test needs a component “iprobe” which is located at the output of the amplifier. It breaks the loop and allows cadence to obtain the Bode for the amplifier as well as the phase margin. With this, we will obtain the amplifier's stability and gain in one simulation. The results can be seen in the graph in Figure 26.

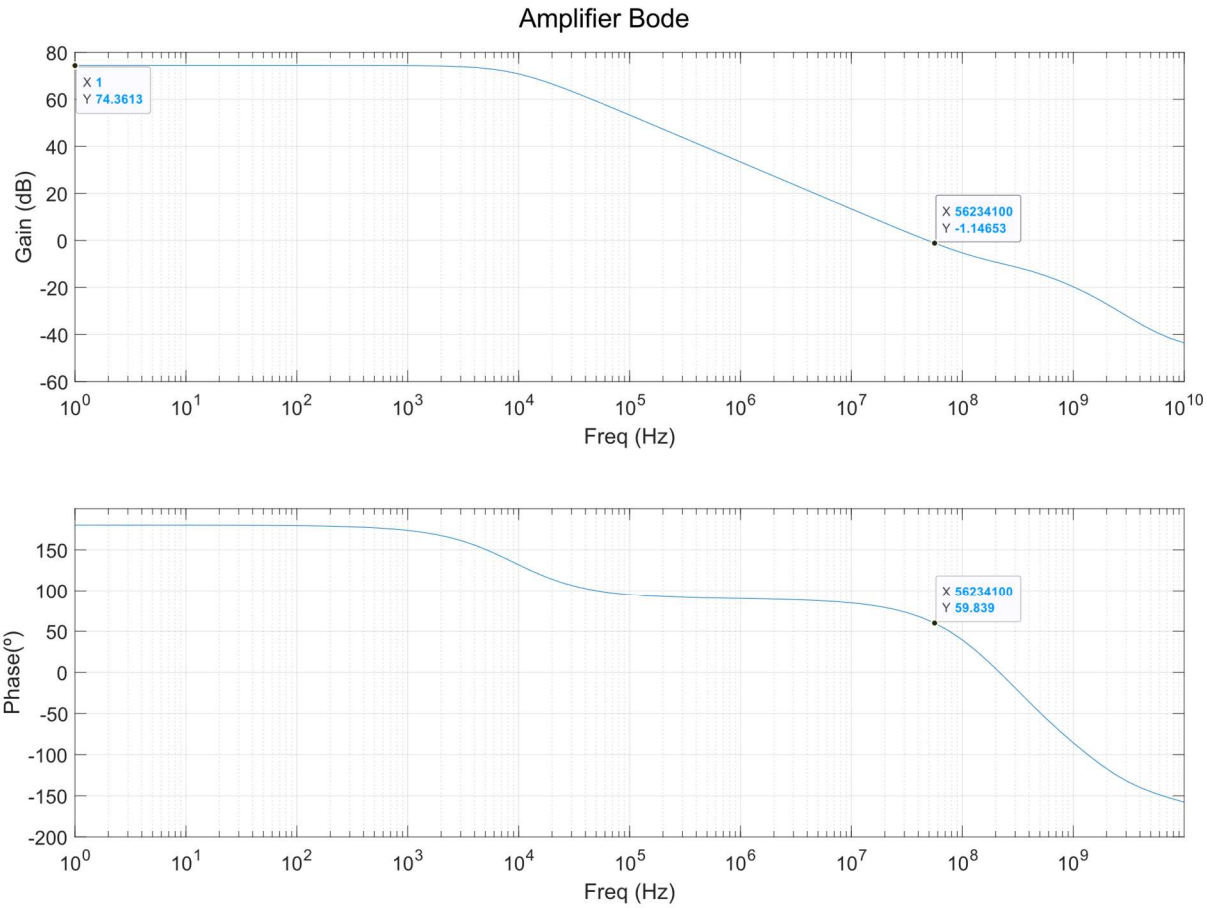


Figure 26. AMPLIFIER BODE FUNCTION

In the graph, we can appreciate the results we wanted to obtain. We first look at the top left data point. This data point indicates the gain value at DC, which is 74 dB greater than the value we were looking for.

Next, we focus on the second data point that checks the frequency at which gain is 0dB, this is, the frequency at which gain is unity, which is the definition of the gain bandwidth product. With this we see that $GBW = 56\ MHz$.

At last, the remaining data point shows the phase of the transfer function when gain reaches unity, which corresponds to the definition of phase margin. Thus, the phase margin, measuring with precision is $PM = 64º$. A value which ensures stability of the system for every other feedback configuration.

We can also appreciate how the effects of the second pole, corresponding to the second stage of the amplifier do not show until the frequency is well over GBW. This indicates that with the Miller capacitance, we have been able to separate poles enough, thus the *GBW* is well modeled by only the effects of the first pole. To correctly model the second pole of the system in this simulation, load capacitance at the output of the amplifier was measured and included as C_{Load}, which can be seen in Figure 25.

We can check the robustness of the design against intradie variations, this introduces mismatch in the transistors. We obtain this by running a Montecarlo simulation. We obtain standard deviations of

$$\sigma_{gain} = 0.223\ dB \quad (54)$$

$$\sigma_{PM} = 0.368\ ° \quad (55)$$

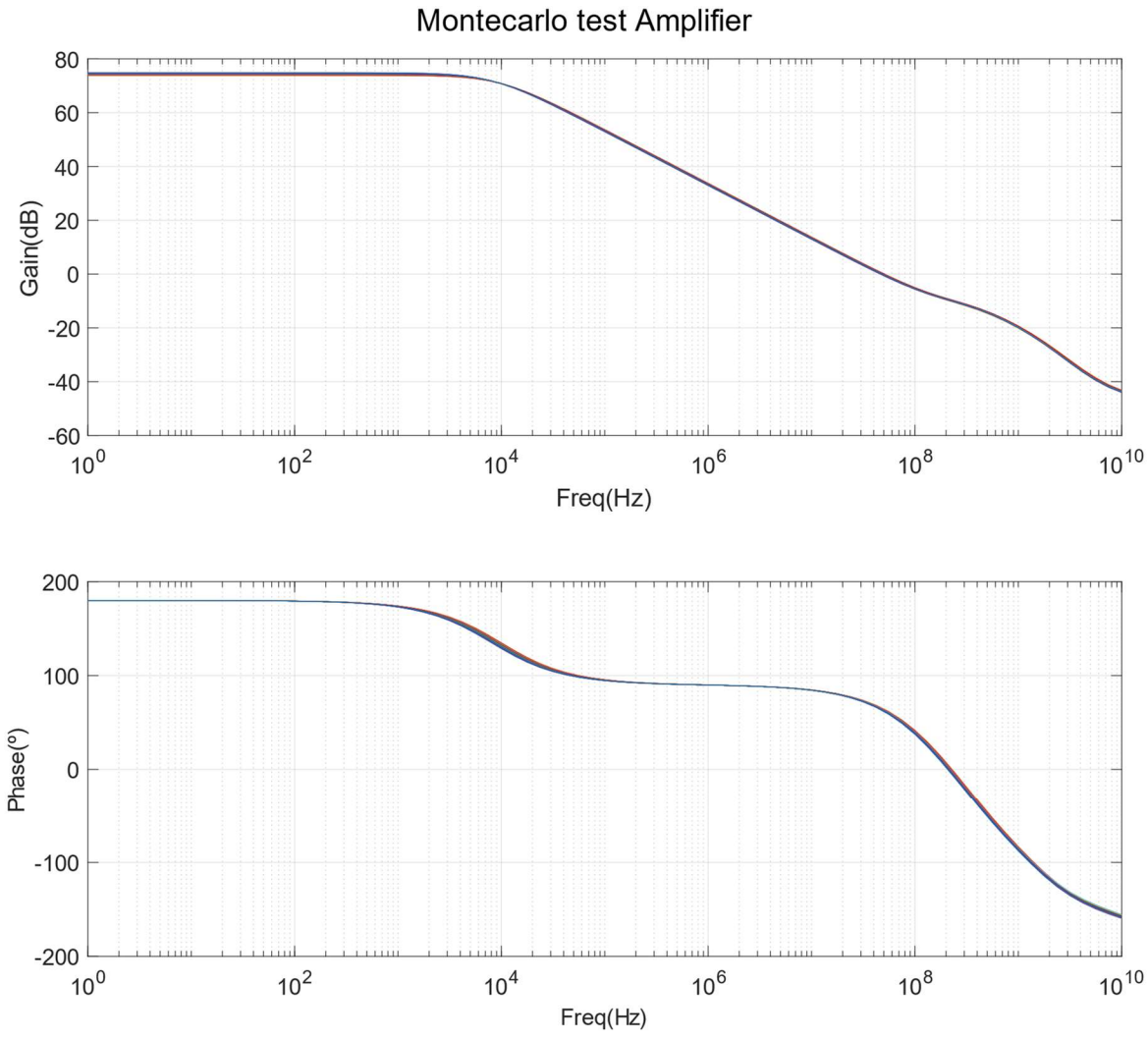


Figure 27. BODE PLOT AMPLIFIER WITH MONTECARLO VARIATIONS

We see this represented in the bode plots of Figure 27. We see that the bandgap design is very resistant to intradie variations, this is thanks to the large area of transistors constituting the design, from Pelgrom's Law we know threshold variations are inversely proportional to the square root of the area WL [19].

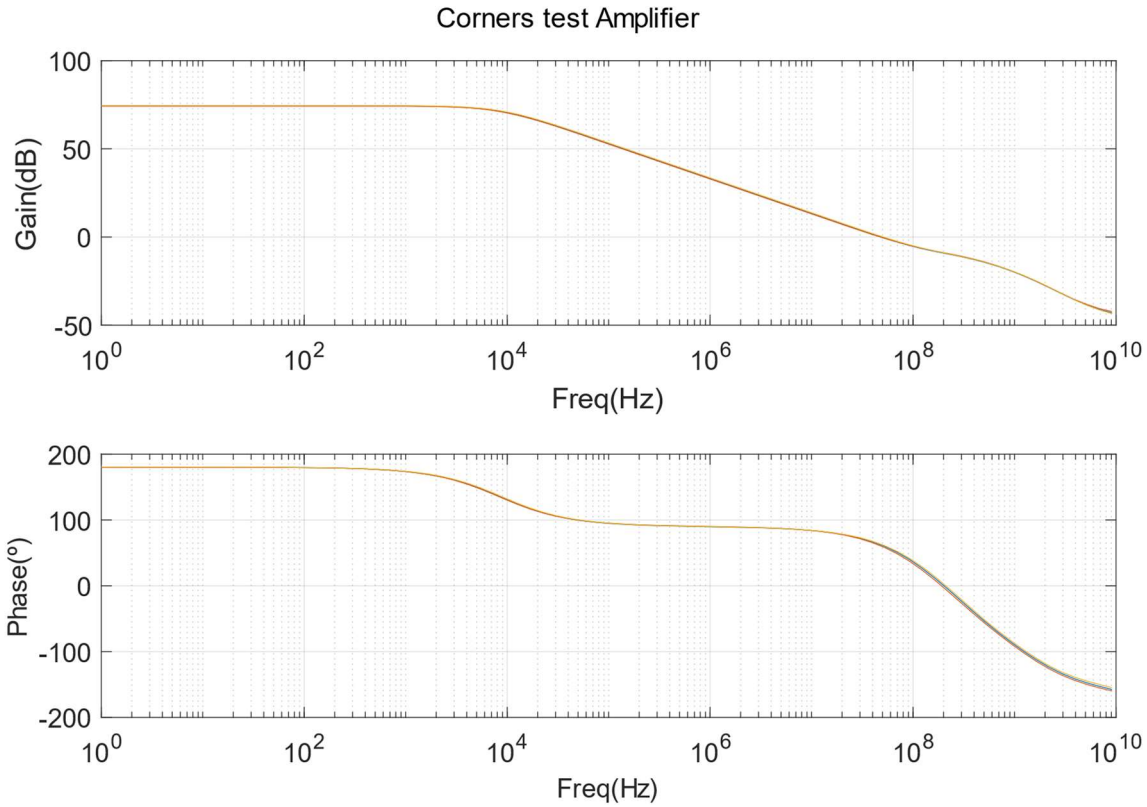


Figure 28. CORNER SIMULATIONS FOR AMPLIFIER

Looking at interdie variations, which are simulated with corner analysis (corners studied were the ones available in the PDK of the technology, these were ff and ss corners), no significant variations can be seen in the graphs which are in Figure 28.

4.2 BANDGAP SCHEMATIC LEVEL SIMULATIONS

With the amplifier completely checked, we can carry on with complete bandgap simulations. These simulations do not require any special configuration as the bandgap is an auto-biased circuit and we only need to connect it to supply voltages. We will perform start-up tests also in this section, as to prove start-up circuit's functionality it needs to activate the bandgap.

We start with a basic test for the nominal behavior of the design. We will measure the variation of voltage with temperature. As a reference for the typical measurement in this kind of circuit, we will use an analysis sweeping temperature from -40ºC to 110ºC as the automobile industry standard [23].

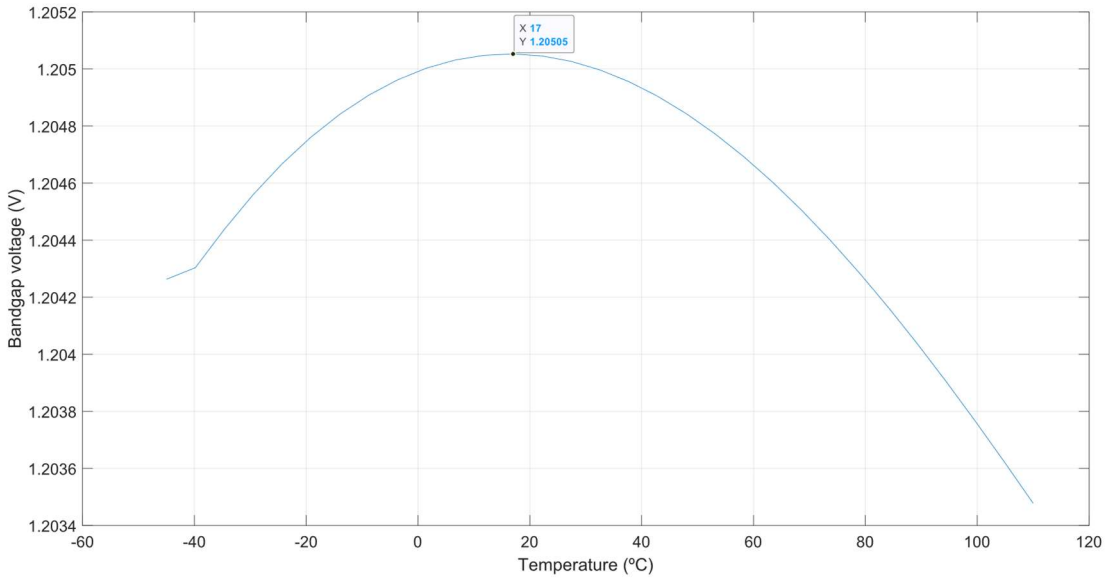


Figure 29. **BANDGAP OUTPUT VOLTAGE VARIATION WITH TEMPERATURE**

We see how the design has a 0-temperature coefficient at approximately 17ºC. We also measure the average temperature coefficient in this range, by measuring the voltage variation from 17ºC to 110ºC, the value is:

$$TC = 1.6882 \cdot 10^{-5}\, V/°C \; = 14.01\, ppm/°C \tag{56}$$

And the nominal value is $V = 1.2\, V$.

We introduce now a ramp-up in the supply voltage to simulate an initialization of the circuit from 0 and check the start-up circuit.

We simulate the transient and the result is seen in the graph in Figure 30. In it we can see that the amplifier's output node correctly establishes itself at the needed value for the bandgap to function correctly and output nominal value.

With this test, we have now checked the correct performance of the nominal design. We have also measured the total power consumption of the circuit, which is

$$P = 587\, \mu W \tag{57}$$

We want to check Montecarlo simulations for mismatch analysis of the bandgap output voltage before we go on with parasitic extraction and results for layout design. We will check how the mismatch between transistors affects the bandgap voltage. Results can be seen in Figure 31.

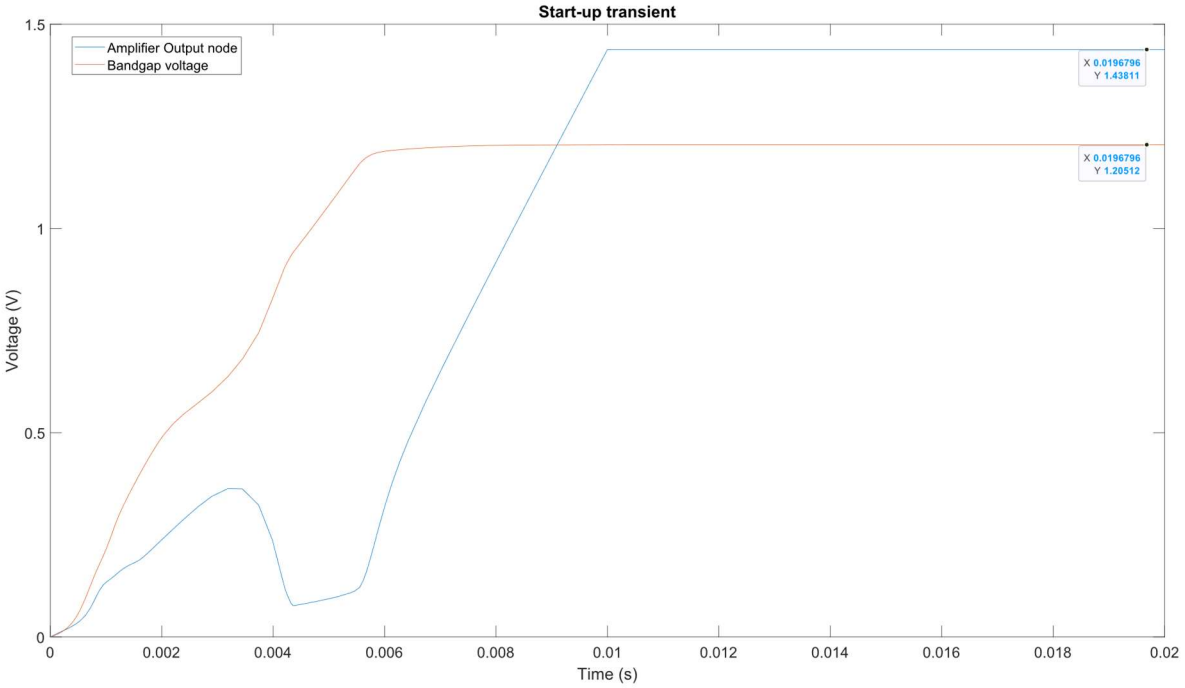


Figure 30. START-UP TRANSIENT RESULTS

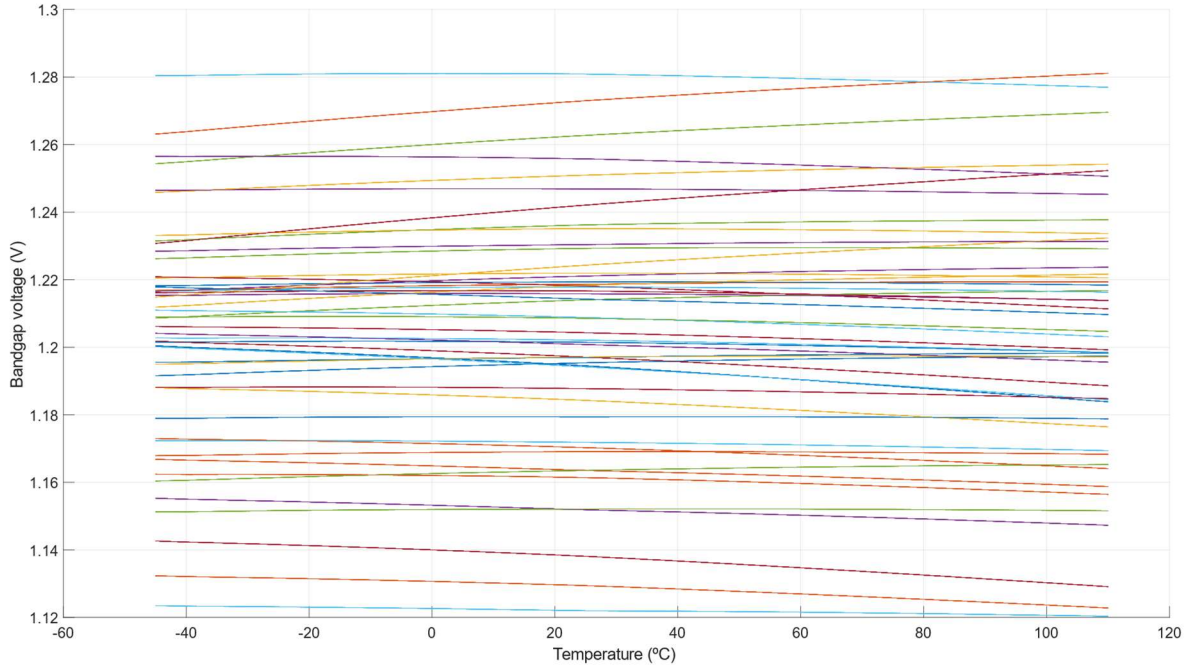


Figure 31. BANDGAP MONTECARLO ANALYSIS

We see big variations as is usual in these circuits. The error in the matching of transistor and resistances translates into a variation of current branches and variations of the PTAT and CTAT temperature coefficients. Although they are still good results, high-performance circuits that demand high precision usually add a trimming mechanism to bandgap circuits to solve variation errors in each circuit. The standard deviation of the nominal voltage value is

$$\sigma_{bg} = 40mV \quad (58)$$

$$\sigma_{TC} = 44ppm/°C \quad (59)$$

The origin of this variation is in the amplifier's input offset, which we can evaluate in simulation. We measure the voltage $V_+ - V_-$ from the input of the amplifier and we obtain with a Montecarlo analysis depicted in the Figure 32.

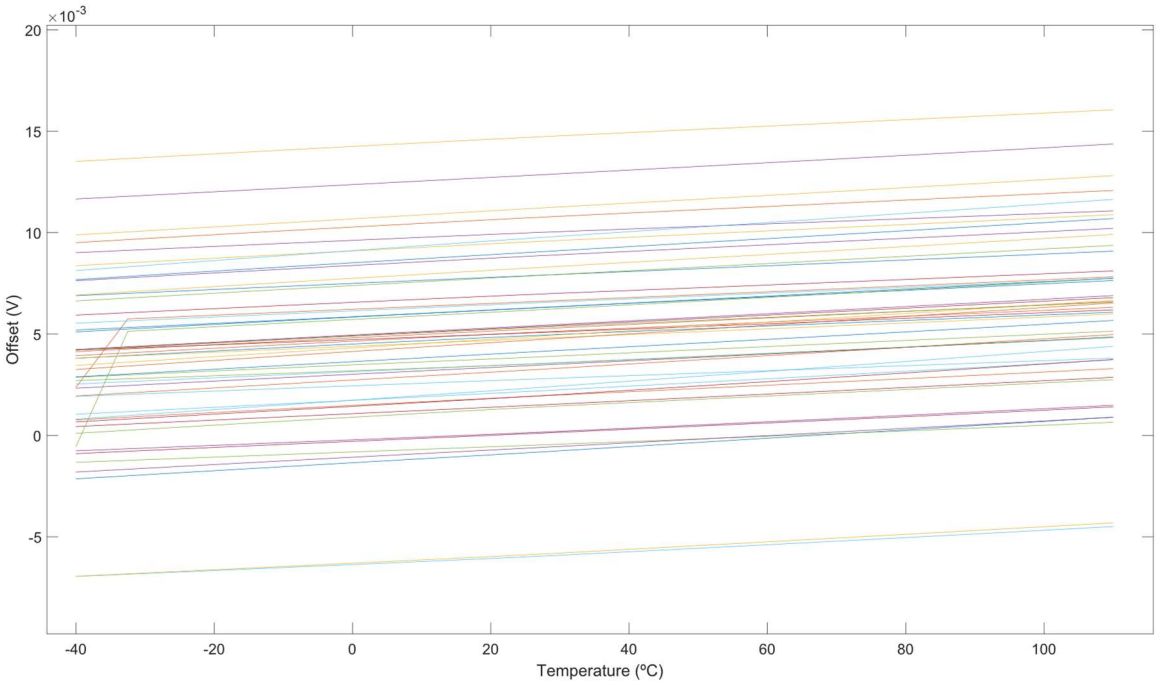


Figure 32. OFFSET MEASUREMENT IN AMPLIFIER'S INPUT

We can observe that even though the amplifier's properties are maintained without significant variation in Figure 27, the imbalance of branch currents inside the amplifier creates a disparity between its inputs which cannot be solved by increasing the size of the amplifier's transistor from this point as is a technology limitation.

Following these tests, we will now measure *PSR* as it was an important design feature -see section 2.2.2. We can observe the transfer function in Figure 33. We can see that it has a very good power supply rejection for low frequencies of -54dB that minimize variations in the output due to supply variations. Coming into

higher frequencies, as the amplifier reaches its bandwidth, it stops rejection variations in supply and PSR comes down until it reaches unity, which means for high frequencies supply variations are directly reflected in the output, as would be expected. Through Montecarlo simulation we can obtain the standard deviation of the PSR factor which is:

$$\boldsymbol{\sigma_{PSR} = 9.85\text{dB}} \quad (60)$$

Finally, we check the noise output for the bandgap. We can see the noise in Figure 34. We see flicker noise contribution in the lower frequencies, and we can observe how noise components decrease with frequency. The total noise in the output of the bandgap can be calculated through integration, obtaining a final noise of $Noise = 1.02mV$. Which gives a signal to noise ratio $SNR \approx 60dB$.

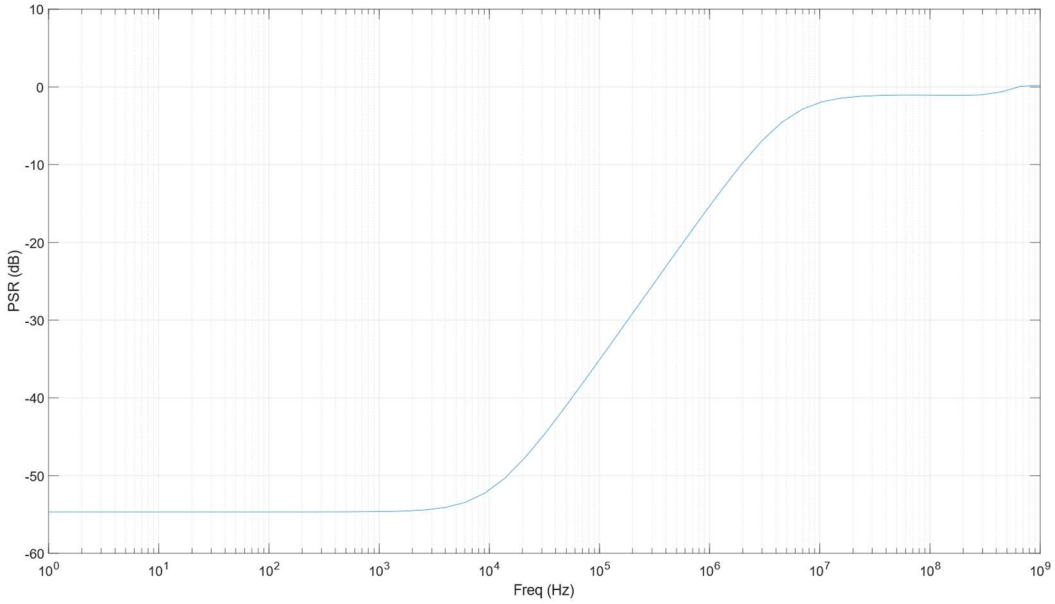


Figure 33. PSR BODE PLOT

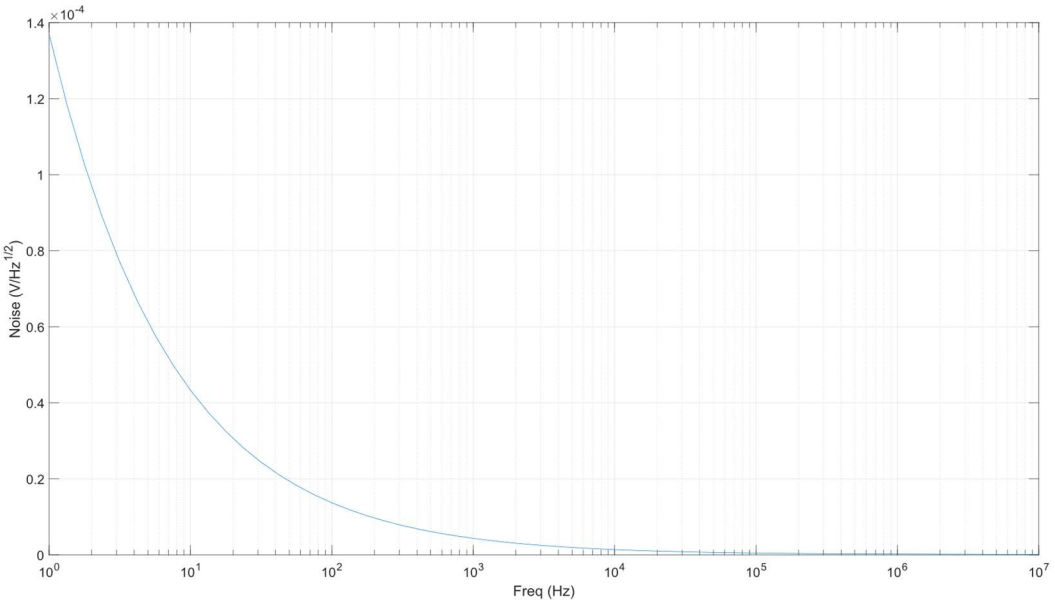


Figure 34. NOISE OUTPUT IN BANDGAP

4.3 LAYOUT AND PARASITIC EXTRACTION SIMULATION

Ultimately, we will extract parasitics of this design and check the same characteristics as the previous section to see if physical design affects to the results.

First, the resistors were calibrated with parasitics to center the device's voltage output at room temperature with parasitics included, and the design is now tested at the complete bandgap system level.

We check first the bandgaps nominal output as the last section in Figure 35.

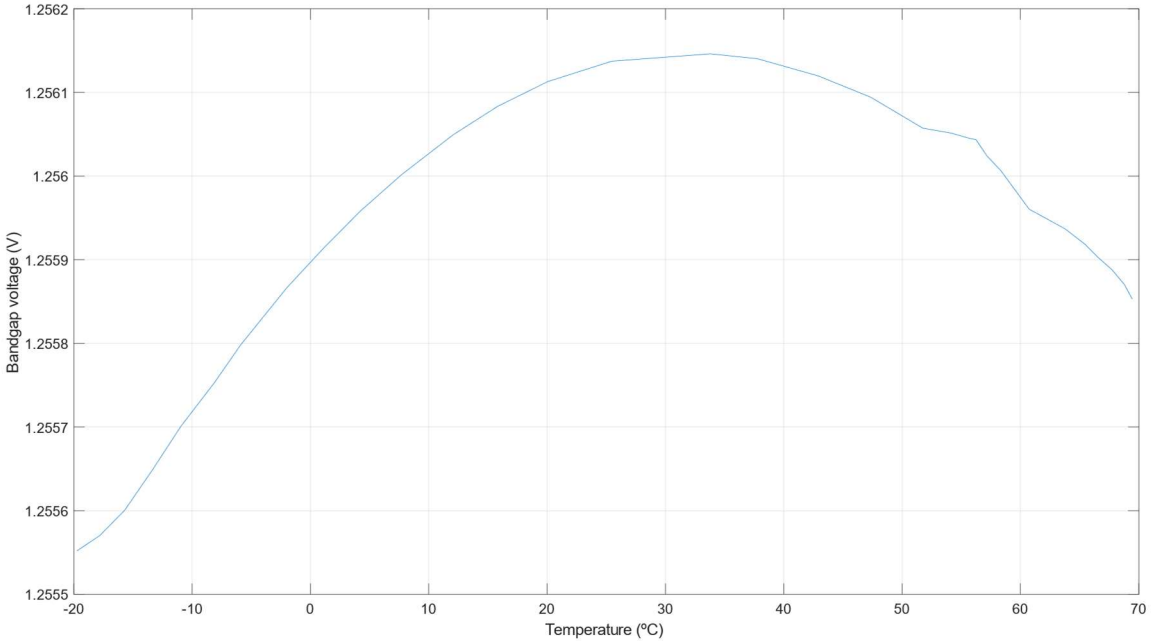


Figure 35. BANDGAP VOLTAGE AFTER PARASITIC EXTRACTION

Voltage level has now shifted to 1.25V. But temperature coefficient cancelation is maintained. We can measure the temperature coefficient from this graph just as in last section and obtain:

$$\boldsymbol{TC = 9.54ppm/°C} \tag{61}$$

A Montecarlo simulation can be done also after the simulation, and we obtain the graph in Figure 36. We can obtain standard deviations for nominal voltage and temperature coefficients.

$$\boldsymbol{\sigma_{Vbg} = 40mV} \tag{62}$$

$$\boldsymbol{\sigma_{TC} = 39.9ppm/°C} \tag{63}$$

The variations of the nominal value of the bandgap voltage are maintained at 40mV, while temperature coefficient is improved with the layout design.

Final tests include the PSR bode after the physical design is implemented. The results obtained are in Figure 37.

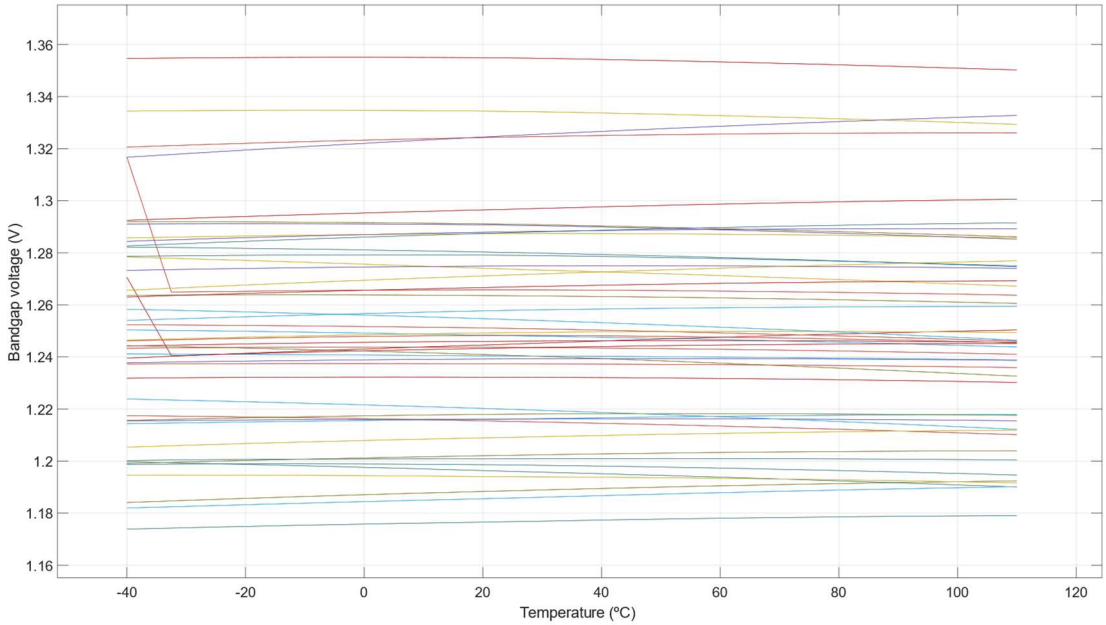


Figure 36. **BANDGAP VOLTAGE MONTECARLO AFTER PARASITIC EXTRACTION**

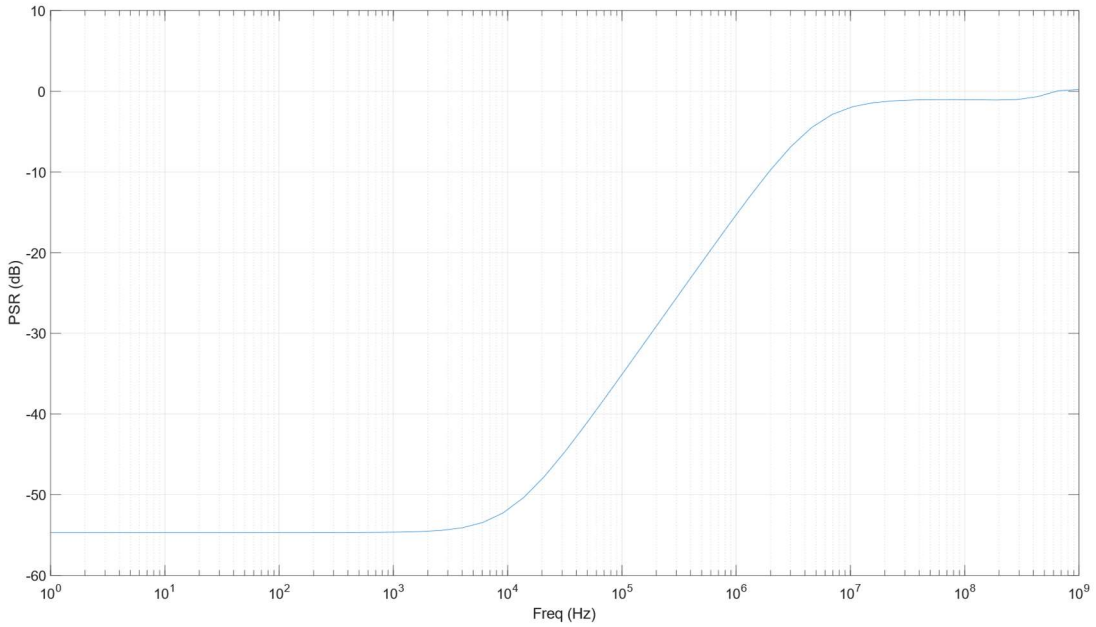


Figure 37. **PSR PLOT AFTER EXTRACTION**

PSR minimum value at $-54dB$ and bandwidth is maintained from previous results but through Montecarlo analysis, we can obtain the standard deviation of this value and obtain:

$$\boldsymbol{\sigma_{PSR(extracted)} = 2.67\text{dB}} \quad (64)$$

The standard deviation of this value is greatly reduced thanks to the physical design of the bandgap. Finally, we obtain the noise figure in Figure 38. Identical to the original figure without parasitic extraction.

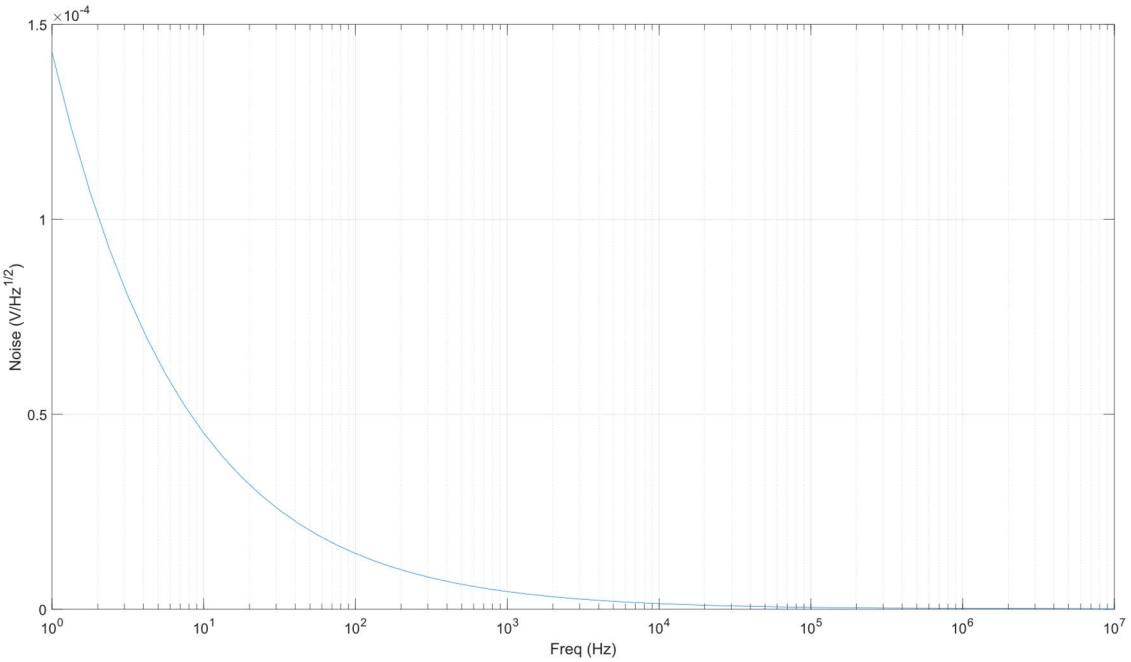


Figure 38. NOISE AFTER LAYOUT DESIGN

We can now compare all results with existing designs we can find in the literature. The comparison can be seen in Table 5.

Table 5. RESULT COMPARISON WITH RESEARCH ARTICLES

Parameters	This work*	[18]	[24]*	[25]
V_{DD} (V)	2.5	1.8	1.7 1.9	1.4 1.5
V_{bg} (V)	1.255	1.086	1.176	0.6
Temperature Range (ºC)	-40 110	-40 125	-40 140	-40 110
TC $(ppm/°C)$	9.54	5-12	13	33
Technology	40nm	160nm	180nm	28nm
Area (mm^2)	0.001	0.12	0.05	0.125
PSR (dB)	-54 @DC	-74 @DC	N.A.	57 @DC
Current (μA)	80	55	50	25
Noise (rms) (mV)	1.02 (1Hz~1GHz)	0.006 (0.1Hz~10Hz)	N.A.	N.A.

*Simulation results

We see the results for this design are very satisfactory, obtaining a reduced area bandgap with state-of-the-art capabilities. These results comply with the requirements needed by the chip it will be implemented in as voltage reference for asynchronous image sensors. The results are compared to a trimmed implementation of the bandgap with variation correction mechanisms [18], a standard bandgap reference implementation [24], and a low voltage implementation in [25]. It is noteworthy the low area demanded by this design which can even be seen compared to lower technological node designs. It achieves an area over ten times lower than the implementations in the designs above mentioned.

4.4 CONCLUSION AND FUTURE WORK

In this work, we have studied the evolution of the bandgap voltage reference structure and reviewed some of the most common up-to-date architectures for them in Chapter 1. We have also presented an in-depth mathematical study of 3 important bandgap parameters such as the PSR, Noise, and stability in Chapter 2. This study has helped then continue with an implementation of the bandgap in Chapter 3 and 4 which has led to a state-of-the-art reduced area bandgap with 1.25V of output voltage.

In conclusion, the design and implementation of the bandgap voltage reference presented in this thesis demonstrate the robustness of the proposed approach in a 40nm node. This design will be fabricated and implemented in a chip. Future work will focus on extensive testing of the fabricated implementation to ensure its stability, reliability, and suitability for integration into mixed-signal systems. The results of these tests will provide valuable insights and potential improvements for the development of more efficient and reliable bandgap voltage references.

Future improvements of this design could be achieved by solving mismatch issues due to intradie variations, as well as reducing noise. This can be done using the chopping technique which solves both issues. Also, resistance trimming can be implemented for fine calibration after fabrication.

This project has enabled me to engage in the comprehensive design of a critical circuit component within the context of a full chip design. Throughout this process, I have navigated all stages of the design procedure, from determining specifications and selecting the most suitable architectures for the project's needs to developing design equations for the target circuit. Concluding the process with the schematic and layout designs, adhering to the previously established criteria. The resulting design was then rigorously tested using appropriate computer-aided software, ensuring its correct functionality upon fabrication. This involvement in the project has helped me settle the knowledge I have acquired in the different subjects coursed in this master’s degree.

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