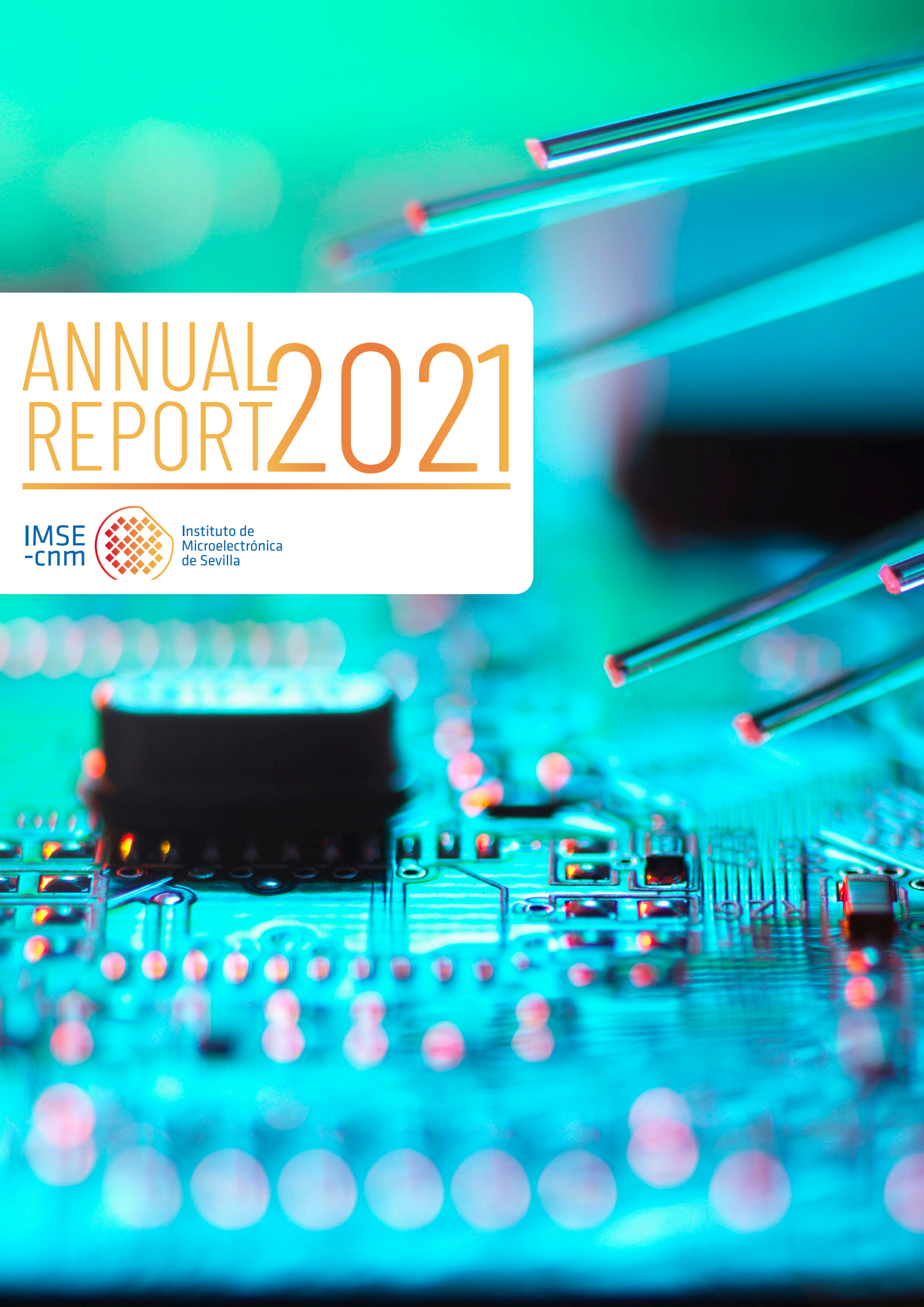
ANNUAL REPORT 2021

IMSE -cnm

Instituto de Microelectrónica de Sevilla



IMSE-cnm Instituto de Microelectrónica de Sevilla

CSIC Consejo Superior de Investigaciones Científicas

Universidad de Sevilla

INSTITUTO DE MICROELECTRÓNICA DE SEVILLA

Centro Nacional de Microelectrónica

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Layour and design: tiporium.com

OUTLINE

FOREWORD

This report summarizes the research activities and the main achieved objectives by the Instituto de Microelectrónica de Sevilla (IMSE) during 2021. This period was marked by slow and progressive recovery from the pandemic. Coronavirus vaccines started to become available and people could slowly return to be physically present at the Institute. After the summer of 2021, CSIC gave instructions to return to full presence, except for special health related cases.

During 2021 the institute had three industrial contracts running, and was granted or initiated one IMSE-coordinated EU project, four national projects, five regional projects, three University of Sevilla projects, one infrastructure project, and nine young employment grants, all totaling 3.6 million euros. Our researchers published 47 international journal papers and filed 2 patents. A total of 3 Ph.D. theses were defended. As a consequence of all this, the Institute reached 100% of the targets set in the CSIC Strategic Plan, particularized with the indicators collected in the PCO (Productivity of Achievement of Objectives).

Overall, 2021 was a good year, with good productivity, as personnel begun to recover from the hit of the pandemic.

ABOUT IMSE

The Instituto de Microelectrónica de Sevilla (IMSE-CNM - Seville Institute of Microelectronics) is an R&D&I joint center of the Consejo Superior de Investigaciones Científicas (CSIC - Spanish National Research Council) and the Universidad de Sevilla. Together with its counterpart institutes in Barcelona and Madrid, it forms part of the Centro Nacional de Microelectrónica (CNM - National Microelectronics Center).

The Institute is dedicated to the field of Physical Science and Technologies, one of the eight areas into which research activity is divided by the CSIC. Its main area of specialization is the design of CMOS analog and mixed-signal integrated circuits and their use in different application contexts such as radio-frequency, microsystems or data conversion.

The IMSE-CNM began its operations in October 1989 under the auspices of an agreement signed by the Junta de Andalucía (the Andalusian Regional Government), the CSIC and the Universidad de Sevilla. Its founding research group was initially based on the premises of the Centro de Informática Científica de Andalucía (CICA – Scientific Computing Center of Andalucía), as a subsidiary department of the Instituto de Microelectrónica de Barcelona (Barcelona Institute of Microelectronics). Later, in 1996, it was established by the Governing Board of the CSIC as a Institute in Formation, occupying a building next to the CICA ceded by the Junta de Andalucía. In late 2008, the Institute was enlarged and relocated in new premises purpose-built by the CSIC in the Parque Científico y Tecnológico Cartuja (Cartuja Scientific and Technological Park). On October 2015, by means of a Specific Collaboration Agreement signed by the CSIC and the Universidad de Sevilla, the center became a Joint Institute of both institutions.

The IMSE-CNM staff consists of approximately one hundred people, including scientists and support personnel. Most of them work for the CSIC and the Universidad de Sevilla. IMSE-CNM employees are involved in advancing scientific knowledge, designing high level scientific-technical solutions and in technology transfer. Their duties include both research and teaching activities, the latter mainly at official master and PhD degrees.

The projects undertaken at the Institute mostly correspond to EU research initiatives, National R+D Plans and Research Plans funded by the Junta de Andalucía. They focus primarily on implementing innovative concepts in silicon, using either the CNM's own clean room at the Instituto de Microelectrónica de Barcelona (IMB-CNM) or external foundries, mainly from Europractice or CMP IC services.

The Institute also participates in several technology and knowledge transfer activities with microelectronics companies, at both national and international level. These activities take the form of collaboration in numerous research contracts, the organization of training courses and the provision of scientific and technical consultation services for companies and government departments.

DIRECTIONS:

The Instituto de Microelectrónica de Sevilla (IMSE) is located in the Parque Científico y Tecnológico Cartuja (Cartuja Scientific and Technological Park) on Isla de La Cartuja, at the corner of Calle Américo Vespucio and Calle Leonardo da Vinci.

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GPS: 37° 24' 44" N - 06° 00' 21" W.

ORGANIZATION

The Instituto de Microelectrónica de Sevilla (IMSE-CNM) is a joint center of the Consejo Superior de Investigaciones Científicas (CSIC - Spanish National Research Council) and the Universidad de Sevilla.

The IMSE-CNM management structure is as follows:

✔**Direction:** Bernabé Linares Barranco
direccion.ims-cnm@csic.es

✔**Vice-Direction:** José Manuel de la Rosa Utrera
jrosa@imse-cnm.csic.es

✔**Technical Vice-Direction:** Joaquín Ceballos Cáceres
joaquin@imse-cnm.csic.es

✔**Management:** José Francisco Barreña Moreno
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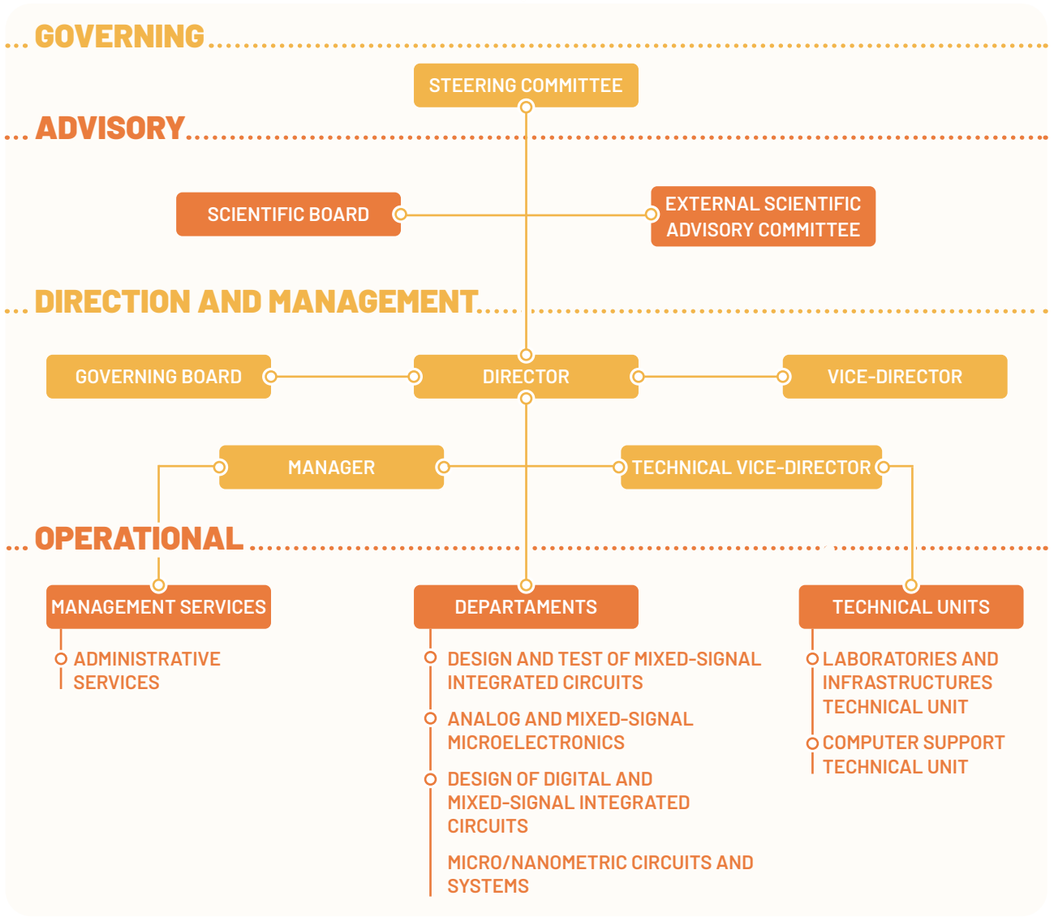


ADMINISTRATIVE SERVICES UNIT

The Institute's research activities are carried out by Research Units responsible for project development. There are currently four of these units:

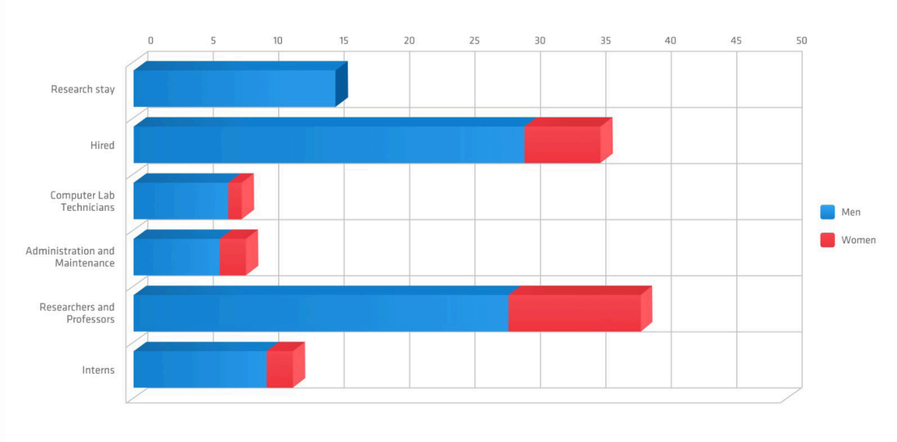
- Design and Test of Mixed-Signal Integrated Circuits
- Analog and Mixed-Signal Microelectronics
- Design of Digital and Mixed-Signal Integrated Circuits
- Micro/Nanometric Circuits and Systems

The Institute's infrastructure is also supported by two Technical Units.

- Laboratories and Infrastructures Technical Unit
- Computer Support Technical Unit

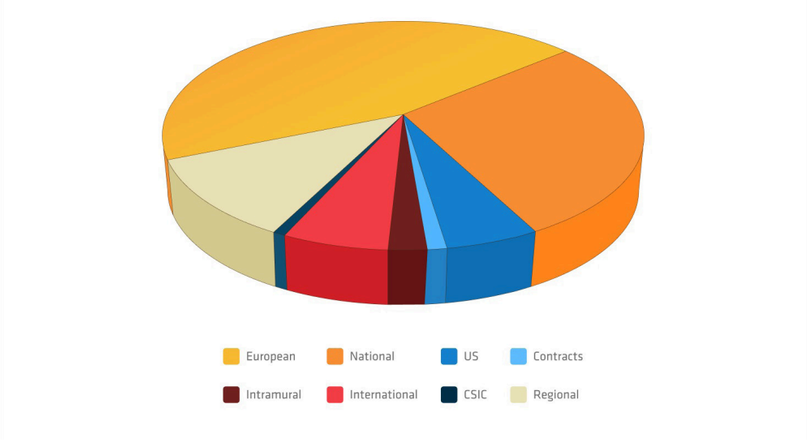
HUMAN RESOURCES

The personnel at the IMSE-CNM permanently or temporarily engaged in the Institute's activities includes nearly 110 people. Most of them work for the CSIC and the Universidad de Sevilla, but there are also teachers and students from other organisms on research internships as it is shown in the figure. These internships do not imply any kind of em ployer-employee relationship with the CSIC



BUDGET

Incoming resources, distributed by concepts, for the year 2021 are shown in the following graphs (excluding staff costs). External funding is obtained either from competitive public projects or industrial contracts. Operating expen ses are provided by CSIC and Universidad de Sevilla.



INFRASTRUCTURE

LABORATORIES

IMSE-CNM has its own laboratories and workshops, specifically habilitated for research, development and innovation tasks carried out at the Institute. The laboratories are well fitted out with equipment and instrumentation, and are run by a permanently employed team of specialists.

Head of Unit

Joaquín Ceballos Cáceres
joaquin@imse-cnm.csic.es >

DEVICE CHARACTERIZATION LAB

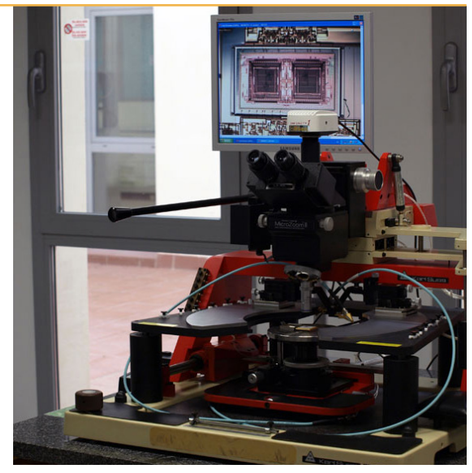
This laboratory is mainly dedicated to perform parametric measurements in semiconductors and passive devices. In this lab it is possible to acquire internal signals from the semiconductors, already cutted and packaged, or from wafers up to 3.5", and performing tests at temperatures ranging from -125ºC to 150ºC.

Chief Lab Technician

Antonio Ragel Morales
ragel@imse-cnm.csic.es

Equipment

Semiconductor Parameter Analyzers, Climatic Cham- bers, Probe Station, Temperature Forcing System, C Meter CV Plotter, LCR Meter.



OPTOELECTRONICS LAB

This lab is equipped with the instrumentation needed to characterize visible light sensors and integrated circuits made up of discrete sensors or visible light matrices. A dark chamber is also available for sensor characterization.

Chief Lab Technician

Antonio Ragel Morales
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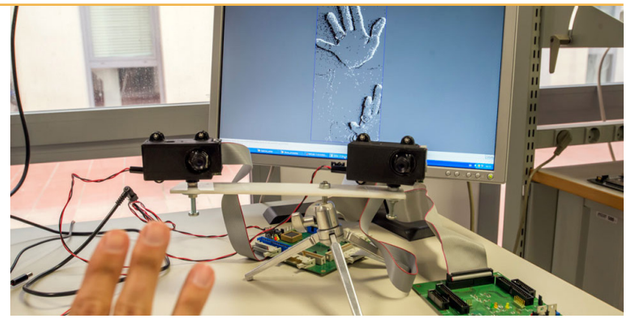

Equipment

Optical Characterization Equipment, Monochromator, Pulsed Laser, Video Development Platform, Lux Meter, Laser Modules, Photo and Video Lenses, Spectrometer

RADIOFREQUENCY LAB

It alllows to perform spectrum and network measurements, and it is equipped with an anechoic chamber for device characterization or electromagnetic compatibility (EMC) measurements. It also allows to perform on wafer (up to 150 mm) as well as on printed circuit measurements.

Chief Lab Technician

Antonio Ragel Morales
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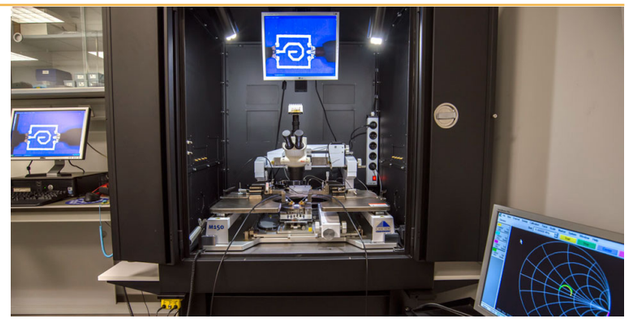

Equipment

Anechoic Chamber, Noise Figure Analyzer, Spectrum/Network Analyzers, Probe Station, Vector Signal Generators, Noise Sources, Power Meter

A/D MEASUREMENT LAB

This is the largest lab in the IMSE. It has twelve fully-reconfigurable mobile stations to carry out the experimental tests on mixed-signal integrated circuits. It also has twelve carts with spectfic measurement equipment that can be attached to any of the mobile stations depending on the requirements of the A/D measurements to perform.

Chief Lab Technician

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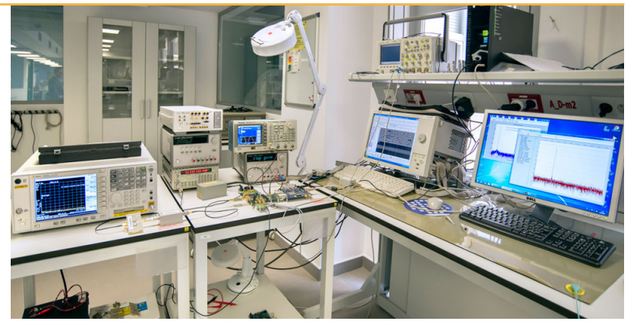

Equipment

Spectrum/Network Analyzers, Logic Analyzers, Arbitrary Waveform Generators, Pulse Generators, Oscilloscopes, Data Acquisition Boards, Differential Amplifiers, Frecuency Counters, Switch/Control Unit, Test Systems, Power Meter, Electrometer, Lock-in Amplifier, Picoammeter, Phase Noise Measurement System.

PULSED LASER LAB

This lab is equlpped with the new pulsed laser PULBOX PICO-RAD compact system for single-event effects testing. Using a single photon technique and a 1064nm wavelength (near-infrared) pulsed laser source, this facility allows the study of the impact of high energy particles over integrated circuits for space, medical or nuclear applications.

Chief Lab Technician

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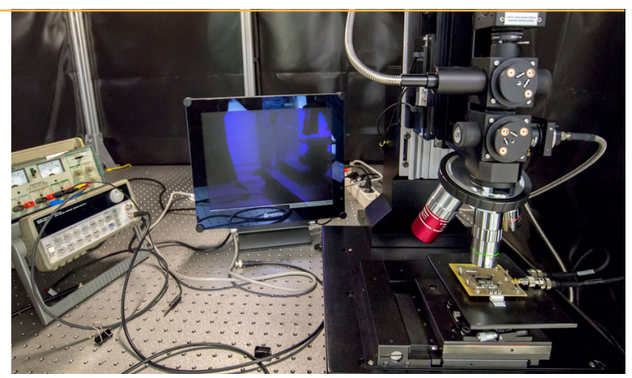

Equipment

Pulsed Laser, Oscilloscope

CIBERSECURITY LAB

The Cibersecurity Laboratory has the required equipment to evaluate the immunity against different types of collateral channel attacks, which are based on the information obtained from the physical implementation of the cryptosystems (power consumption, algorithm's execution time, response to induced failures, electromagnetic emission, etc.).

Chief Lab Technician

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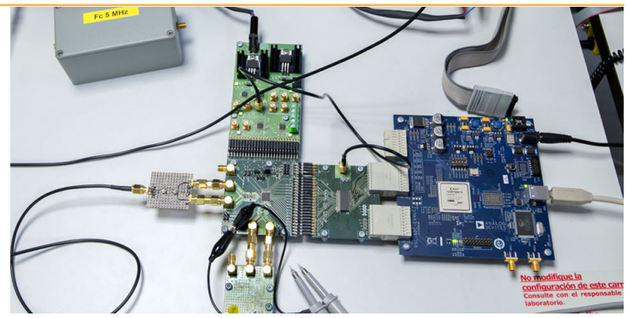

Equipment

Device Current Waveform Analyzer, Logic Analyzers, Function Generators, Pulse Generators, Oscilloscopes, Arbitrary Waveform Generator, Power Meter, Motorized XY Microscope Stage, Ultra Wide Band Low Noise Amplifier, Data Acquisition System, Power Supply

COMPLEX SYSTEMS LAB

This lab has been designed to provide accommodation to those systems that, due to either their size or their special characteristics, require a greater space or an isolated environment. It is also equipped with a showcase for the manipulation of dangerous chemical products and a security cabinet.

Chief Lab Technician

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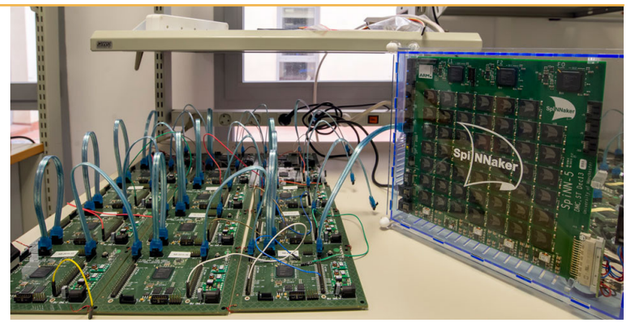

Equipment

Koala Robot, Area Preparation System, 3D Printer

ATE AGILENT 93000

The Agilent 93000 SOC C200e Semiconductor Test System allows carrying out prototyping and fabrication tests of mixed-signal circuits (either already packaged or directly onto the wafer) in one only platform. It is also posslble to incorporate the Thermonics T-2650 BV, a temperature forcing system that allows to perform the tests under temperature conditions ranging from -55ºC to 200ºC.

Chief Lab Technician

José M. Mora Gutiérrez
jmiguel@imse-cnm.csic.es

Equipment

Agilent 93000 Semiconductor Test System, Temperature Forcing System, Oscilloscope

SPECIAL ASSEMBLY WORKSHOP

The Special Assembly Workshop has equipment for soldering and desoldering high density packaging components, such as BGAs, mini-BGAs and fine-pitch surface-mount components

Chief Lab Technician

Miguel A. Lagos Florido
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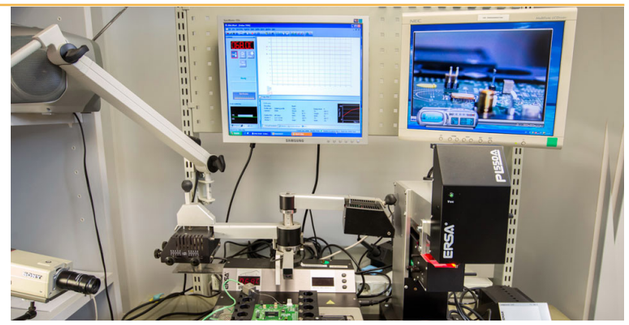

Equipment

IR Rework System, Precision Placement System, Soldering Stations

PACKAGING WORKSHOP

This workshop is devoted to make the bonding between chip and package. It has all the required resources to face the challenges that deep-submicron technologies pose, allowing connections with pitch sizes down to 50 µm. This workshop features two semi-automatic ultrasound micro-soldering machines, with thread diameters of up to 17 µm, for ball-bonding and wedge-bonding. To verify the quality of connections, there is a micro-soldering test system for evaluating thread-resistance and solder ball shear. It also has two chip and wafer storage units for keeping ICs at optimal temperature and humidity conditions.

Chief Lab Technician

Manuel Repiso
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Equipment

Wire Bonders, Bondtester, Ultra Low Humidity Cabinets

PCB ASSEMBLY WORKSHOP

The PCB Assembly Workshop has all the equipment needed for soldering and desoldering thru-hole circuits mounted on PCBs, perforated matrix plates, and, in general, on any circuit-test development plates that do not require special welding techniques.

Chief Lab Technician

Manuel Repiso
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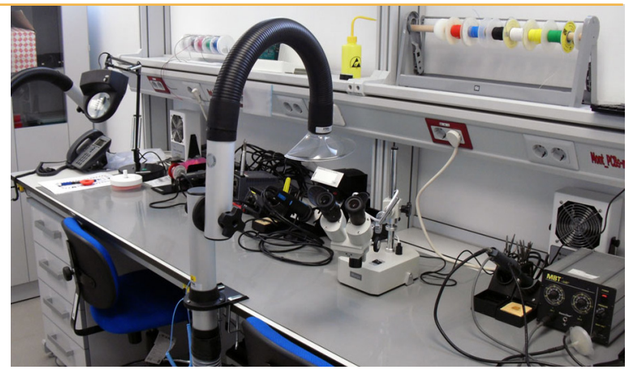

Equipment

Soldering & Desoldering Stations, Ultrasonic Cleaning Bath

◆ CAD TOOLS

Most of the software tools used at the IMSE-CNM are design tools which cover several stages of the integrated circuit design process, from automatic HDL-based synthesis to the completion of full-custom layouts. As a member of the European consortium EUROPRACTICE, IMSE-CNM holds many of the licenses required by these design tools. The CAD software tool library at IMSE-CNM also includes in-house CAD tools and free-distribution tools from universities and other research centers.

CAD Manager

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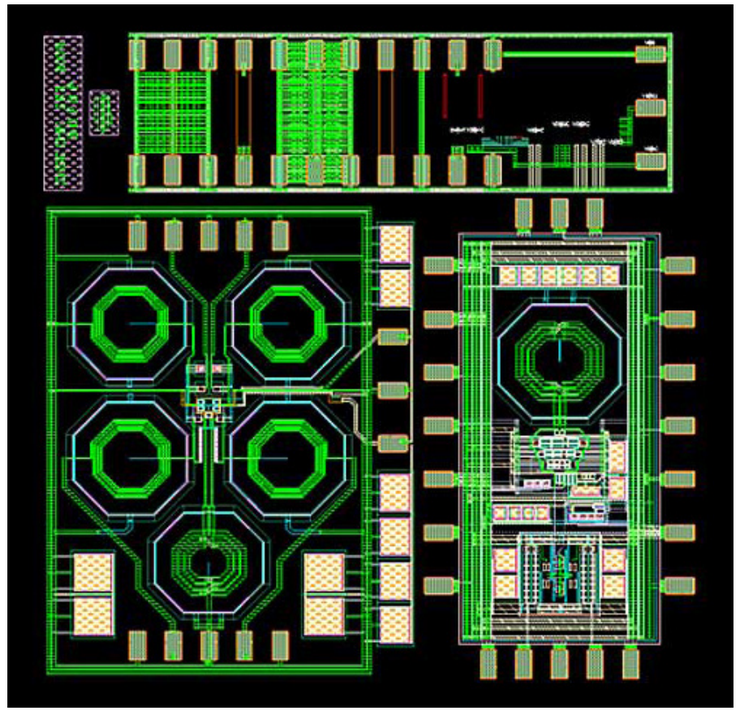

◆ COMMERCIAL TOOLS

CADENCE DESIGN FRAMEWORK II

Analog and digital semi/full-custom design.

Cadence provides a complete integrated circuit environment allowing both analog design flows (schematic capture, electrical simulation, layout editing, design rule checking, parasitic extraction, LVS verification, etc.) and digital flows (functional description, automatic synthesis, logic simulation, automatic place & route, etc.). The environment also includes tools and languages for describing and simulating mixed analog-digital designs (AHDL, hierarchy editor, etc.).

MENTOR GRAPHICS

Analog and digital semi/full-custom design.

Mentor Graphics provides a complete integrated circuit environment allowing full digital design flow (functional description, automatic synthesis, logic simulation). This tool also covers semi-custom and full-custom layout design.

SYNOPSYS

Simulation and VHDL synthesis.

Synopsys provides a series of HDL simulation and synthesis tools (VHDL and Verilog) for designs in both ASIC and FPGA technologies. The current distribution of this tool includes also packages for high-level synthesis, low-power synthesis, design for testability, test files and test vector generation, formal verification, temporal analysis and the use and development of IP modules.

XILINX

FPGAs development.

Xilinx provides different tools for FPGA system design: Integrated Software Environment (ISE), a basic set of tools that facilitates the description, synthesis, implementation and verification of designs created on Xilinx CPLDs and FPGAs; Embedded Development Kit (EDK) for programmable embedded system design; ChipScope Pro, which makes it possible to

display all the signals and internal nodes of an FPGA; and System Generator for DSP, for developing digital signal processing systems on FPGAs.

SABER

Electrical simulator for mixed-signal designs.

Among other utilities, this includes: SaberHDL, a tool for simulating complex mixed-signal systems or technologies; SaberDesigner, for creating and editing designs, controlling simulations interactively and displaying and analyzing waveforms; SaberGuide, for behavioral simulation; SaberSketch, a graphical user interface; and MAST, a mixed-signal hardware description language.

HSPICE

Electrical simulator.

The standard tool for simulating circuits at electrical level, this simulator makes it possible to incorporate certified device models from leading MOS device manufacturers. Featuring latest-generation simulation and analysis algorithms, it has become one of the most reliable and best known industrial circuit simulators.

AGILENT ADVANCED DESIGN SYSTEM

Design tool for high frequency design.

The Advanced Design System (ADS) is an electronic design automation tool for RF, microwave and signal integrity applications. It uses cutting edge technologies such as 3D EM and X-parameter simulators. This tool is used by leading developers of wireless applications for communications and networks, and also by leading aerospace and defense technology companies. In one single integrated platform ADS provides design and verification standards, with wireless design libraries and EM circuit-system co-simulation, for WiMAX, LTE, multi-gigabit links and radar and satellite communications applications.

MATLAB/SIMULINK

High-level technical computing language and interactive prototype design and development. Dynamic and embedded multi-domain simulation environment. MATLAB is a high-level technical computing language and an interactive platform for algorithm design, numerical computation and data analysis and visualization. Simulink is a tool for multi-domain simulation and design based on dynamic and embedded system models.

IN-HOUSE CAD TOOLS

XFUZZY

Design of fuzzy-inference systems

Xfuzzy, the design environment for fuzzy systems, includes a set of tools that help with the design of fuzzy-logic inference-based systems, from initial description right through to final implementation. Based on the XFL specification language, Xfuzzy has tools for describing, verifying and synthesizing fuzzy systems (both software and hardware). It also features tools which allow the easy editing of package operators and hierarchical structures, tools for generating 2-D and 3-D data graphics and tools for monitoring inference processes.

FRIDGE

Circuit optimization using simulated annealing techniques

FRIDGE is an analog circuit optimization tool with many innovative features. It was developed to streamline the process of designing integrated circuits. FRIDGE is used to size analog circuits automatically according to design requirements. The optimization process takes place in two stages: in the first, statistical optimization techniques are applied, while deterministic techniques are applied in the second. Computational costs are drastically reduced by correctly formulating the cost function (where the designer's requirements are established) and adjusting the movement generator to match the nature of the analog sizing problem. All this can be done thanks to FRIDGE's innovative features, which include: preliminary exploration of the design space using a coarse grid to determine the best regions for further exploration, adaptive control of the temperature in the simulated annealing statistical techniques, synchronization of movement amplitude in parameter space with the temperature, etc.

SIMSIDES

SIMulink-based SIgma-DElta Simulator

SIMSIDES is a time-domain behavioral simulator for ∑ΔMs that was developed as a toolbox in the MATLAB/SIMULINK environment. SIMSIDES can be used for simulating any arbitrary ∑ΔM architecture implemented with discrete-time (DT) or continuous-time (CT) circuit techniques.

RESEARCH AREAS & LINES

The Instituto de Microelectrónica de Sevilla is structured into Research Units whose scientific objectives focus primarily on the implementation and experimental verification of innovative concepts related to the design of micro- and nano-electronic circuits and systems.
The Research Lines developed at IMSE-CNM aim to provide solutions both in traditional sectors, such as communications, processing systems or instrumentation, and in emerging sectors, such as medical engineering, environment or space technology. These lines also consider the introduction of new devices, such as nano-sensors and micro-electro-mechanical systems (MEMS), and the use of unconventional computing paradigms, such as neural networks or fuzzy logic.

RESEARCH AREAS

ANALOG SIGNAL PROCESSING
- Analog, Mixed-Signal and Radio Frequency (AMS-RF) Circuits
- Analog-to-Digital Converters and Mixed-Signal Interfaces
- T est and Design-for-Test of Analog, Mixed-Signals and RF (AMS-RF) Circuits
- Modeling, Design and Synthesis Techniques of Analog, Mixed-Signal, RF and Heterogeneous Circuits and Systems
- Low-Voltage and Low-Power Analog and Mixed-Signal Design in Deep Submicron and Nanometer CMOS Technologies
- Sigma-Delta Data Converters

DIGITAL SIGNAL PROCESSING & VLSI SYSTEMS
- CMOS Digital Intelligent and Suistainable Integrated Circuits
- DigItal Embedded Systems and IoT
- Cybersecurity

BRAIN-INSPIRED NEURAL NETWORKS AND ARTIFICIAL INTELLIGENCE
- Neuromorphic Cognitive Systems
- Microelectronic Systems for Computational Intelligence

SENSORY & PHOTON IC VISION SYSTEMS
- CMOS Smart Imagers and Vision Chips
- Heterogeneous Sensory-Processing Systems and 3-D Integration
- Dynamic Vision Sensors

NANOELECTRONICS AND EMERGING TECHNOLOGIES
- Circuit Design using Emerging Devices and Non-Conventional Logic Concepts
- Nanoscale Memristor Circuits and Systems

BIOMEDICAL AND BIOINSPIRED CIRCUITS AND SYSTEMS
- Biomedical Circuits and Systems
- Wireless Implantable and Wearable Intelligent Biosensor Devices

INTEGRATED CIRCUITS FOR SPACE APPLICATIONS
- High-Speed High-Resolution ADCs & DACs for Space

RESEARCH AREA ◆ ANALOG SIGNAL PROCESSING

Analog, Mixed-Signal and Radio Frequency (AMS-RF) Circuits

Contact

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The activities of this research line focus on the development of design techniques and methodologies, mainly in advanced CMOS technologies, for analogue mixed-signal and radiofrequency circuits, with special emphasis on analogue-digital converters (ADCs) and application specific IPs (intellectual properties) for front-end analogue signal processing applications that require low power consumption, high speed and high resolution. We develop concepts such as robustness against technological variability and environmental conditions, digital calibration, self-correction and self-adjustment. All this in the framework of systems for different applications, and specifically for aerospace and wireless communications applications.

Keywords
Analog Design; Analog-to-Digital Converters; Radio Frequency Front-End; Digital Calibration; Self-Correction; Wireless and Space Applications

Research Highlights

◆ J.L. Gonzalez, J.C. Cruz, R.L. Moreno and D. Vazquez, "A Proposal for Yield Improvement with Power Tradeoffs in CMOS LNAs", IEEE Latin America Transactions, vol. 14, no. 1, pp. 13-19, Jan 2016 »

◆ R. Fiorelli and E. Peralías, "Semi-empirical RF MOST model for CMOS 65nm technologies: Theory, extraction method and validation", Integration, the VLSI Journal, vol. 52, pp. 228-236, 2016»

◆ A. Ginés, R. Fiorelli, A. Villegas, R. Doldán, M. Barragán, D. Vázquez, A. Rueda and E. Peralías, "Design of an Energy Efficient ZigBee Transceiver", Chap. 7 in Thomas Noulis (Ed.), Mixed-signal circuits, CRC-Press, 2015 »

◆ A.J. Ginés, G. Leger, E. Peralías and A. Rueda, "Close-loop Simulation Method for Evaluation of Static Offset in Discrete-Time Comparators", Proceeding of the IEEE International Conference on Electronics Circuits and Systems (ICECS), Marsella, 2014 »

◆ R. Fiorelli, F. Silveira and E. Peralias, "MOST Moderate-Weak-Inversion Region as the Optimum Design Zone for CMOS 2.4-GHz CS-LNAs", IEEE Transactions on Microwave Theory and Techniques, vol. 62, no. 3, pp. 556-566, 2014 »

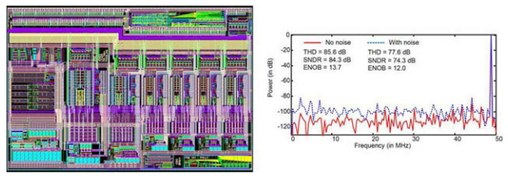
Key Research Projects & Contracts

n-PATETIC: New paradigms for testing mixed-signal integrated circuits (TEC2015-68448-R)
PI: Adoración Rueda Rueda
Funding Body: Min. de Economía y Competitividad
Jan 2016 - Dec 2018

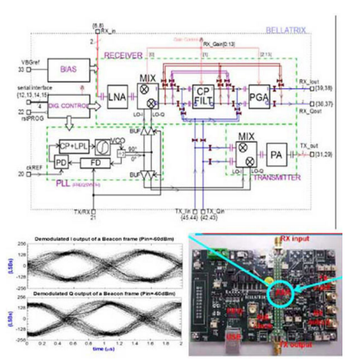
DANTE: Adapting Mixed-signal and RF ICs Design and Test to Process and Evironment Variability (TEC2011-28302)
PI: Adoración Rueda Rueda
Funding Body: Min. de Ciencia e Innovación
Jan 2012 - Dec 2015

ACATEX: Self-calibration and self-test of analog, mixed-signal and radio frecuency circuits (P09-TIC-5386)
PI: Adoración Rueda Rueda
Funding Body: Junta de Andalucía - Proyectos de Excelencia
Mar 2010 - Feb 2014

SR2: Short Range Radio (2A105- Catrene) (TSI-020400-2008-71 and TSI-020400-2010-55) » web
PI: Adoración Rueda Rueda
Funding Body: Catrene European Program y MITyC Programa Avanza+
Jan 2008 - Dec 2011



Caption: 1.8V 15-bit 100Msps Pipeline ADC: layout and post-layout simulation results of Nyquist performance with and without transient noise



Caption: Prototype of a Zigbee/IEEE 802.15.4 transciever, implemented in a 1.2V 90nm CMOS technology

Analog-to-Digital Converters and Mixed-Signal Interfaces

Contact

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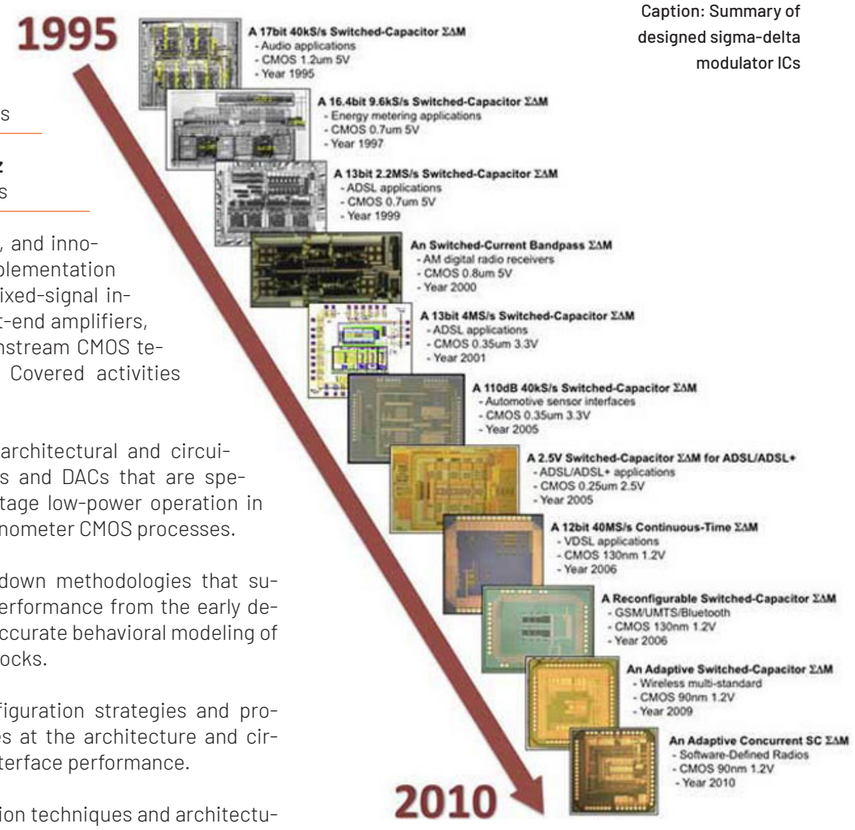


Caption: Summary of designed sigma-delta modulator ICs

Research, development, and innovation regarding the implementation of high-performance mixed-signal interfaces, including front-end amplifiers, ADCs and DACs, in mainstream CMOS technological processes. Covered activities include:

- Exploration of novel architectural and circuital techniques for ADCs and DACs that are specially suited for low-voltage low-power operation in deep-submicron and nanometer CMOS processes.

- Development of top-down methodologies that support their optimized performance from the early design phases, including accurate behavioral modeling of mixed-signal circuital blocks.

- Exploration of reconfiguration strategies and programmability techniques at the architecture and circuit level for adaptive interface performance.

- Exploration of calibration techniques and architectures.

- Optimum chip implementation and verification.

The areas of application include wireline, wireless and optoelectronic communications, sensor interfaces, and medical electronics.

Expertise is supported by a long-term tradition (over 20 years) in the field of mixed-signal design, with special emphasis on sigma-delta, pipeline, ramp and SAR ADCs and several chips successfully transferred to industry. The accumulated know-how drives R&D, cooperation, and dissemination activities with both academia and world-leader industrial partners.

Keywords
ADCs; DACs; Mixed-Signal Interfaces; Nyquist; Sigma-Delta; Pipeline; SAR; Current-Steering; Design Methodologies; Behavioral Modeling; Performance Pptimization

Technology Transfer

Transference of a high-performance sigma-delta converter designed by our research group to Alcatel Microelectronics and STMicroelectronics for its incorporation into the ADSL2+ modem chipset ST20190 Utopia for CPE applications (massive production in 2004).

Research Highlights

◆ J. Ruiz-Amaya, M. Delgado-Restituto and A. Rodriguez-Vazquez, "Device-Level Modeling and Synthesis of High-Performance Pipeline ADCs", Springer, 2011

◆ R. del Rio, F. Medeiro, B. Perez-Verdu, J.M. de la Rosa and A. Rodriguez-Vazquez, "CMOS Cascade Sigma-Delta Modulators for Sensors and Telecom: Error Analysis and Practical Design", Springer, 2006

◆ J. Ruiz-Amaya, J.M. de la Rosa, F.V. Fernandez, F. Medeiro, R. del Rio, B. Perez-Verdu and A. Rodriguez-Vazquez, "High-Level Synthesis of Switched-Capacitor, Switched-Current and Continuous-Time ∑Δ Modulators using SIMULINK-Based Time-Domain Behavioral Mo-

dels", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 52 (9), pp. 1795-1810, 2005

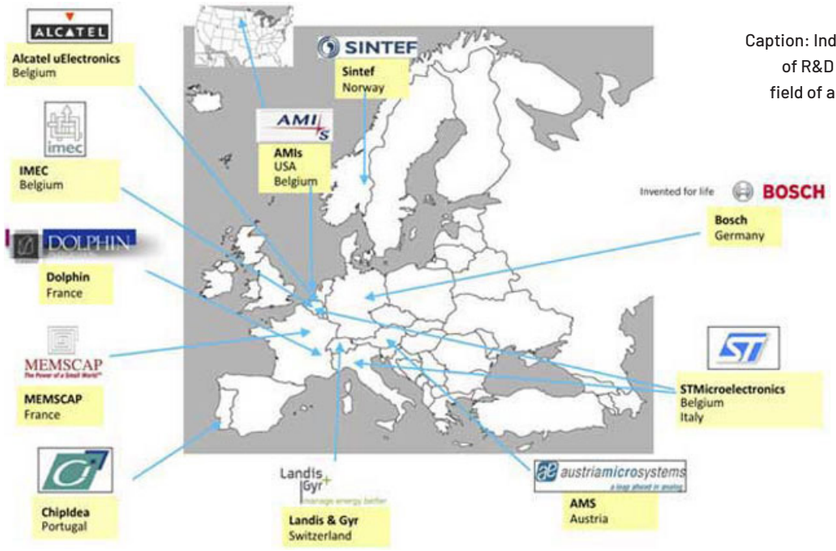
◆ A. Rodriguez-Vazquez, F. Medeiro and E. Janssens (Eds.). "CMOS Telecom Data Converters", Springer, 2003

Key Research Projects & Contracts

SPIRIT: Secured Platform for Intelligent and Reconfigurable Voice and Data Terminals (MEDEA+ 2A101)
PI: Manuel Delgado Restituto
Funding Body: MEDEA+ (European public funding)
2006 - 2009

TAMES-2: Testability of Analog Macrocells Embedded into System-on-Chip (IST 2001-34283)
PI: Belén Pérez Verdú
Funding Body: European Union (European public funding)
2002 - 2004

Design of Up-Stream and Down-Stream Data Converter for New Generation ADSL6
PI: Ángel Rodríguez Vázquez
Funding Body: Alcatel Microelectronics (European private funding) 2001 - 2003



Caption: Industrial partners of R&D activities in the field of analog-to-digital interfaces

Test and Design-for-Test of Analog, Mixed-Signals and RF (AMS-RF) Circuits

Contact

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Gildas Léger
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This research line gathers all the activities related to the development of test techniques. These can be low-cost functional approaches whose goal is the direct estimation of the specified performance. Other structural approaches (defect-oriented or indirect) make more use of Design-for-Testability features and rely on the consideration that the circuit is correct by design. As a result, they are more focused on the detection of spot defects or unexpectedly excessive parametric deviations.
In both cases, embedded test techniques (commonly called Built-In Self-Test or BIST) are of particular interest to reduce test plan complexity, to enable the test of IP blocks with limited accessibility within a System-on-Chip (SoC) or even to enable in-field testing (which increases system-level diagnosis capability).
Our most recent research themes in this line are:

- On-line test and BIST for AMS-RF circuits.

- Characterization techniques for periodic signals and signal generation circuits for the embedded functional test of AMS circuits.

- Low-cost functional test techniques for Analog to Digital data converters.

- Machine-learning indirect test applied to AMS-RF circuits.

- Development of robust tests based on causal relationships.

Keywords
Mixed-Signal Integrated Circuits; Test; Testing; Design-for-Test (DfT); Built-In-Selft-Test (BIST); Machine-Learning

Research Highlights

◆ G. Leger and M. J. Barragan, "Brownian distance correlation-directed search: A fast feature selection technique for alternate test", Integration, the VLSI Journal, vol. 55, pp. 401–414, Sep 2016

◆ A.J. Gines E. Peralias, G. Leger, A. Rueda, G. Renaud, M.J. Barragan and S. Mir, "Linearity test of high-speed high-performance ADCs using a self-testable on-chip generator", IEEE European Test Symposium (ETS), Amsterdam, 2016

◆ M.J. Barragan and G. Leger, "A Procedure for Alternate Test Feature Design and Selection", IEEE Design & Test, vol. 32, no. 1, pp. 18–25, Feb 2015

◆ M.J. Barragan, G. Leger, D. Vazquez and A. Rueda, "On-chip sinusoidal signal generation with harmonic cancelation for analog and mixed-signal BIST applications", Analog Integrated Circuits and Signal Processing, vol. 82, pp. 67-79, 2015

◆ Best Special session award: M.J. Barragan, G. Leger, F. Azais, R.D. Blanton, A. D. Singh and S. Sunter, "Special session: Hot topics: Statistical test methods," VLSI Test Symposium (VTS), Napa (USA), 2015

Key Research Projects & Contracts

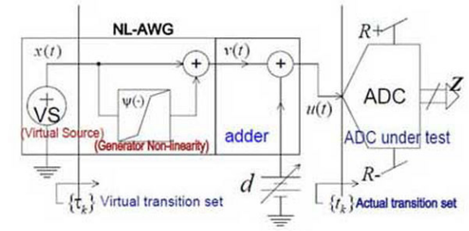
IndieTEST: Indirect Test solutions for analog, mixed-signal and RF integrated systems (PICS CNRS)
PI: Gildas Léger (CSIC) / Manuel Barragán (CNRS)
Funding Body: CSIC & CNRS
Jan 2017 - Dec 2019

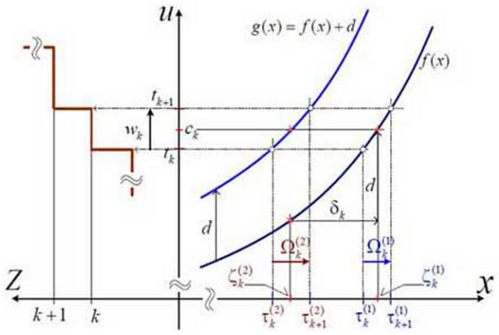
n-PATETIC: New paradigms for testing mixed-signal integrated circuits (TEC2015-68448-R)
PI: Adoración Rueda Rueda
Funding Body: Min. de Economía y Competitividad
Jan 2016 - Dec 2018

DANTE: Adapting Mixed-signal and RF ICs Design and Test to Process and Evironment Variability (TEC2011-28302)
PI: Adoración Rueda Rueda
Funding Body: Min. de Ciencia e Innovación
Jan 2012 - Dec 2014

ACATEX: Self-calibration and self-test of analog, mixed-signal and radio frecuency circuits (P09-TIC-5386)
PI: Adoración Rueda Rueda
Funding Body: Junta de Andalucía - Proyectos de Excelencia. Mar 2010 - Feb 2014

TOETS: Towards One European Test Solution
PI: José L. Huertas Díaz
Funding Body: CE: CATRENE European Program - CT302. Dec 2009 - Nov 2011





Caption: Statistical post processing for Alternate Test. From a completely characterized subset of circuits, a machine-learning algorithm extracts the non-linear and multi-dimensional relations between simple signatures and specifications. This model is further used to test the rest of circuits with the simple signatures only.

Measurement method] Caption: Measurement method for ADCs based on double-histogram. From the histograms (output code density) obtained for a non-linear monotonous input signal and its replica with an additive offset, the INL of a high-resolution ADC can be retrieved at low cost.

Modeling, Design and Synthesis Techniques of Analog, Mixed-Signal, RF and Heterog neous Circuits and Systems

Contact

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The general objective of this research line is to develop new modeling, design and synthesis strategies for analog, mixed-signal, radio-frequency (RF) and heterogeneous integrated circuits and systems, aiming at better performances, smaller design and fabrication cost and smaller power consumption. This also involves dealing with the increasing variability of modern technologies.
More specifically, the work includes activities in different aspects of the circuit design flow, as well as their exploitation in industrial-class designs:

- Pareto-based behavioral modeling with support to multiple hierarchical design flows.

- Layout-aware synthesis methodologies for analog/RF circuits.

- Electromagnetic-simulation-based performance modeling of passive devices for RF circuit design.

- Variability-aware design techniques.

- Development and exploitation of emerging design methodologies: bottom-up techniques, hybrid techniques and competitive strategies.

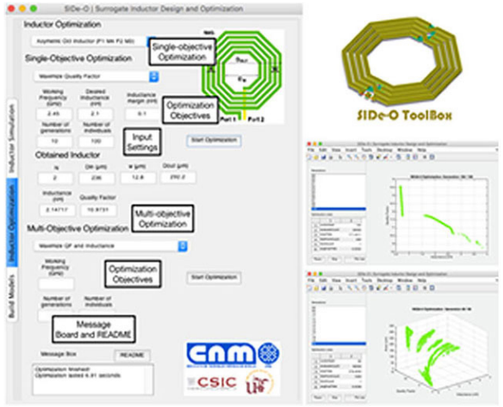
- Simulation techniques for time-zero and time-dependent variability.

Keywords
Systematic Design Methodologies; Single-Objective and Multi-Objective Optimization; Reconfigurable Design; Layout-Aware Design; Variability-Aware Design; Aging Simulation

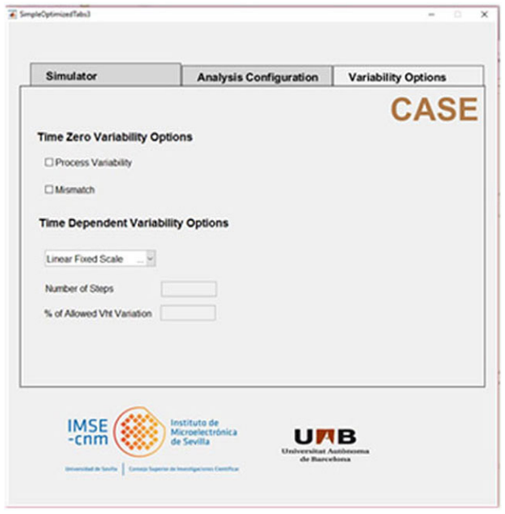
Research Highlights

◆ F. Passos, E. Roca, J. Sieiro, R. Castro-Lopez and F.V. Fernandez, "An Efficient Transformer Modeling Approach for mm-Wave Circuit Design", AEU - International Journal of Electronics and Communications, vol. 128, article 153496, 2021

◆ F. Passos, E. Roca, R. Martins, N. Lourenço, S. Ahyoune, J. Sieiro, R. Castro-Lopez, N. Horta and F. V. Fernandez, "Ready-to-Fabricate RF Circuit Synthesis using a Layout- and Variability-Aware Optimization-based Methodology", IEEE Access, vol. 8, pp. 51601-51609, 2020



Caption: Design Tool developed in the group: SIDe-O Toolbox



Caption: Design Tool developed in the group: CASE

◆ F. Passos, E. Roca, J. Sieiro, R. Fiorelli, R. Castro-Lopez, J.M. López-Villegas and F.V. Fernandez, "A multilevel bottom-up optimization methodology for the automated synthesis of RF system", IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems, vol. 39, no. 3, pp. 560-571, 2020

◆ A. Toro-Frías, P. Martín-Lloret, J. Martin-Martinez, R. Castro-López, E. Roca, R. Rodriguez, M. Nafria and F.V. Fernández, "Reliability simulation for analog ICs: Goals, solutions, and challenges", Integration - the VLSI Journal, vol. 55, pp. 341-348, 2016

◆ R. Castro-Lopez, O. Guerra, E. Roca and F.V. Fernandez, "An Integrated Layout-Synthesis Approach for Analog ICs", IEEE Trans. on Computer-Aided Design, vol. 27, no. 7, pp. 1179-1189, 2008

Key Research Projects & Contracts

VIGILANT: The Variability Challenge in Nano-CMOS - SUBPROJECT MITIGATION (PID2019-103869RB-C31)
PI: Francisco V. Fernández Fernández / Rafael Castro López
Funding Body: Min. de Ciencia, Innovación y Universidades
Jun 2020 - May 2023

TOGETHER: Towards Trusted Low-Power Things: Devices, Circuits and Architectures (TEC2016-75151-C3-3-R)
PI: Francisco V. Fernández Fernández / Rafael Castro López
Funding Body: Min. de Economía, Industria y Competitividad
Jan 2017 - Jun 2021

MARAGDA: Multilevel approach to the reliability-aware design of analog and digital integrated circuits (TEC2013-45638-C3-3-R) » web
PI: Francisco V. Fernández Fernández
Funding Body: Min. de Economía y Competitividad
2014 - 2018

KIT-LTCC: Design Kit Development in LTCC ceramic technology: modeling, simulation and fabrication of components and circuits, and design methodology (RTC-2014-2426-7)
PI: Elisenda Roca
Funding Body: Min. de Economía y Competitividad
Sep 2014 - Jan 2017

AMADEUS: Analog Modeling and Design Using a Symbolic Environment (ESPRIT IV 21821)
PI: Francisco V. Fernández Fernández
1996 - 2000

Low-Voltage and Low-Power Analog and Mixed-Signal Design in Deep Submicron and Nanometer CMOS Technologies

Contact

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Ángel Rodríguez Vázquez
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This research line embraces all activities related to the conception and design of basic building blocks and mixed-signal subsystems for system-on-chip implementation in CMOS nanometric technologies. Emphasis is placed on topologies and methods for low-voltage operation with very low power consumption. This is a transversal line whose activities intersect and provide support to the other research lines of the group. Typically building blocks and subsystems are designed for inclusion into chips implementing different system-level functions. Activities in this line include:

- Conception of new topologies for analog and mixed-signal building blocks suitable for deep submicron technologies.

- Modeling of second-order phenomena for these topologies. Embodiment of these models to support analog design flows.

- Development of design plans aimed to achieving high-performance with minimum power budget.

- Identification and exploration of fundamental limits and scaling performance of these building blocks.

- Exploration of architectural solutions for low-power operation, including power optimization, power management, smart stand-by control, etc.

- Conception of optimum architectural solutions for block programmability, error correction and calibration.

- etc.

All application areas are covered, namely, from low-noise sensor interfaces to high-frequency communications. All major analog and mixed-signal functions embedded into systems are explored. The group has been active in analog and mixed-signal design since the late eighties and through these years have devised many different kind of building blocks for smart imaging chips, automotive sensors, wireline and wireless communications, RFID, neuro-fuzzy adaptive systems, etc.

Keywords
Analog and Mixed-Signal Circuits; Synthesis, Modeling and Design; Low-Voltage; Ultra Low-Power; High-Frequency; Communications; Sensor Interfaces; Calibration

Research Highlights

◆ J.A. Rodriguez-Rodriguez, M. Delgado-Restituto, J. Masuch, A. Rodriguez-Perez, E. Alarcon and A. Rodriguez-Vazquez, "An Ultralow-Power Mixed-Signal Back End for Passive Sensor UHF RFID Transponders", IEEE Transactions on Industrial Electronics, vol. 59, no. 2, pp. 1310-1322, 2012

◆ A. Rodriguez-Perez, J. Ruiz-Amaya, M. Delgado-Restituto and A. Rodriguez-Vazquez, "A Low-Power Programmable Neural Spike Detection Channel with Embedded Calibration and Data Compression", IEEE

Transactions on Biomedical Circuits and Systems, vol. 6, no. 2, pp. 87-100, 2012

◆ J.A. Rodriguez-Rodriguez and M. Delgado-Restituto, "A low-power baseband processor for passive RFID tags employing low-power design techniques", in A.N. Laskovski (Ed.), Advances in RFID Tags, InTech, 2011

◆ J. Ruiz-Amaya, M. Delgado-Restituto and A. Rodriguez-Vazquez. "A 1.2V 10-Bit 60-MS/s 23mW CMOS Pipeline ADC with 0.67pJ/Conversion-Step and Onchip Reference Voltage Generator", Analog Integrated Circuits and Signal Processing, vol. 71, no. 3, pp. 371-381, 2011

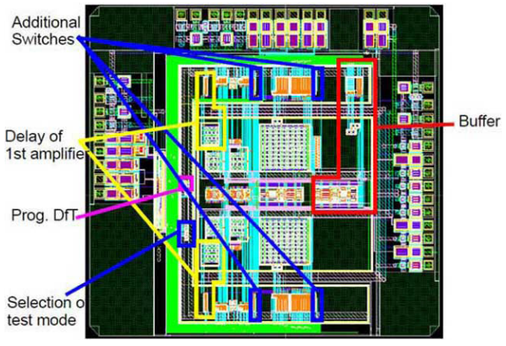
◆ J. Fernandez-Berni, R. Carmona-Galan, F. Pozas-Flores, A. Zarandy and A. Rodriguez-Vazquez. "Multi-Resolution Low-Power Gaussian Filtering by Reconfigurable Focal-Plane Binning", Proc. SPIE 8068, Bioelectronics, Biomedical, and Bioinspired Systems V; and Nanotechnology V, 806806, Prague, Czech Republic, 2011

Key Research Projects & Contracts

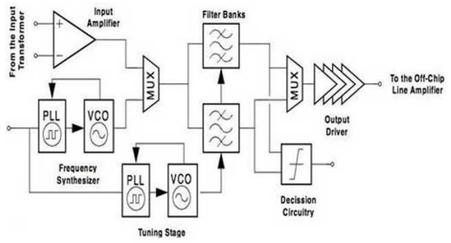
AFLS4K: Diseño micro-electrónico de un sensor lineal de alta velocidad para aplicaciones de inspección de procesos industriales (0619/0076)
PI: Óscar Guerra Vinuesa
Funding Company: Innovaciones Microelectrónicas
2009

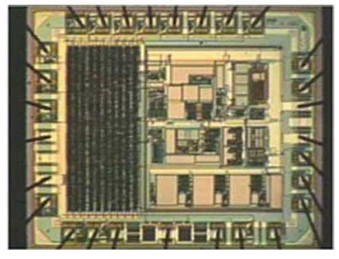
BIOTAG: Monolithic Implementation of Passive RFID Transponders for Biomedical Applications (TIC-02818)
PI: Manuel Delgado Restituto
Funding Body: Proyectos de Excelencia, Junta de Andalucía
2008

MIXMODEST: Mixed Mode In Deep Submicron Technologies (ESPRIT-29261)
PI: Ángel Rodríguez Vázquez
Funding Body: Otros Programas, Organismos Públicos Europeos
1998



Caption: Test Cirtuitry for High-Resolution ADCs





Caption: A Mixed-Signal CMOS Modem ASIC for Data Transmission on the Low-Voltage Power Line

Sigma-Delta Data Converters

Contact

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This research line deals with the analysis, modeling, design, implementation and experimental characterization of Sigma-Delta Modulators (SDMs) integrated in nanometer CMOS technologies. Different application scenarios are considered, spanning from sensor interfaces to broadband wireless communications. A number of Integrated Circuits (ICs) have been (and are being) developed, considering several circuit techniques, namely: discrete-time (switched-capacitor and switched-current), continuous-time (active-RC, Gm-C, Gm-LC) and hybrid continuous-time/discrete-time circuits

The research activities carried out in the last five years have been focused on the design of SDMs intended for wireless communications, software defined radio and IoT devices. In these topics, several state-of-the-art IC prototypes have been designed in cutting-edge nanometer CMOS technologies. The design of these ICs has been supported and fueled by design methodologies and CAD tools, specifically developed to systematize the synthesis and verification procedure and to optimize the performance in terms of target specifications with minimized power consumption. An example of these CAD tools is SIMSIDES, a time-domain behavioral simulator for SDMs developed in the MATLAB/SIMULINK environment. Since the first version of SIMSIDES was developed in 2003, the tool has been continuously updated and improved with new models and facilities, and has been distributed to a number of universities, research institutes and companies all over the world.
More details can be found in www2.imse-cnm.csic.es/~jrosa

Keywords
Sigma-Delta Modulators; Analog-to-Digital Converters; Oversampling Analog-to-Digital Converters; RF-to-Digital Sigma-Delta Converters; Sigma-Delta Radio Receivers; Behavioral Modeling, Simulation and Optimization

Research Highlights

◆ J.M. de la Rosa and R. del Río, CMOS Sigma-Delta Converters: Practical Design Guide, Wiley-IEEE Press, 2018
M. Honarparvar, J.M. de la Rosa, F. Nabki and M. Sawan, "SMASH Delta-Sigma Modulator with Adderless Feedforward Loop Filter", IET Electronics Letters, vol. 8, pp. 532-534, 2017

◆ J.M. de la Rosa, R. Schreier, K.P. Pun and S. Pavan, "Next-Generation Delta-Sigma Converters: Trends and Perspectives", IEEE J. on Emerging and Selected Topics in Circuits and Systems, vol. 5, pp. 484-499, 2015

◆ G. Molina-Salgado, A. Morgado, Gordana Jovanovic-Dolecek and J.M. de la Rosa, "LC-based Bandpass Continuous-Time Sigma-Delta Modulators with Widely Tunable Notch Frequency", IEEE Trans. on Circuits and Systems - I: Regular Papers, vol. 61, pp. 1442-1455, 2014

◆ J.M. de la Rosa, "Sigma-Delta Modulators: Tutorial Overview, Design Guide and State-of-the-Art Survey", IEEE Trans. on Circuits and Systems I: Regular Papers, pp. 1-21, 2011

Key Research Projects & Contracts

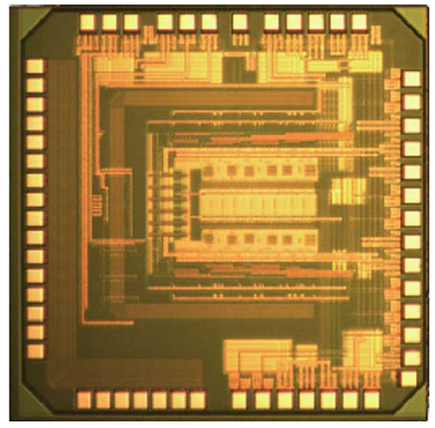
CORDION: Cognitive Radio Digitizers for IoT (PID2019-103876RB-I00)
PI: José M. de la Rosa Utrera
Funding Body: Min. de Ciencia e Innovación
Jun 2020 - Jun 2023

NEURO-RADIO: Cognitive Radio with embedded Neural Learning (US-1260118)
PI: Luis A. Camuñas Mesa / José M. de la Rosa Utrera
Funding Body: Junta de Andalucía
Jan 2020 - Jan 2022

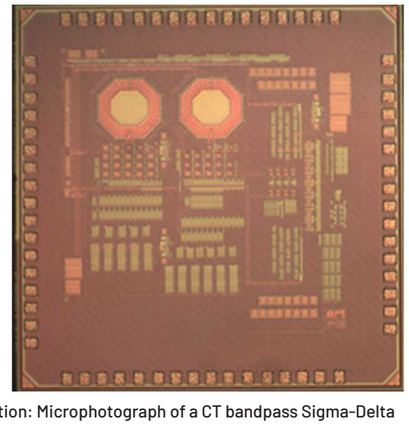
TOGHETHER: Towards Trusted Low-Power Things: Devices, Circuits and Architectures (TEC2016-75151-C3-3-R)
PI: Francisco V. Fernández Fernández & Rafael Castro López
Funding Body: Min. de Economía, Industria y Competitividad
Dec 2016 - Dec 2019

FENIX-SDR: Flexible Nanometer CMOS Analog Integrated Circuits for the Next Generation of Software-Defined-Radio Mobile Terminals (TEC2010-14825/MIC)
PI: José M. de la Rosa Utrera
Funding Body: Min. de Ciencia e Innovación
Jan 2011 - Dec 2013

ARAMIS: Adaptive RF and Mixed-signal Integrated Systems for 4G Wireless Telecom (TEC2007-67247-C02-00/MIC)
PI: José M. de la Rosa Utrera
Funding Body: C.I.C.Y.T.
Oct 2007 - Sep 2010



Caption: Microphotograph of a programmable SC lowpass cascade Sigma-Delta Modulator for SDR applications, implemented in a 90-nm CMOS technologyModulator for RF digitization, implemented using Gm-LC circuits in a 65-nm CMOS technology



Caption: Microphotograph of a CT bandpass Sigma-Delta Modulator for RF digitization, implemented using Gm-LC circuits in a 65-nm CMOS technology

RESEARCH AREA ◆ DIGITAL SIGNAL PROCESSING & VLSI SYSTEMS

CMOS Digital Intelligent and Suistainable Integrated Circuits

Contact

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This research topic has as main aim the efficient implementation of digital integrated circuits on ASICs at several abstraction levels: at a transistor level, designing basic digital cells with a full-custom methodology; at a gate level, finding optimum solutions for combinational and sequential circuits; at a circuit level, developing architectures and timing strategies. Transversal optimization mechanisms are employed in all these implementations, such as for instance, switching activity analysis, minimization of power consumption, low switching-noise generation, design of cells with data-independent power consumption, design for high-speed applications, etc.
Work in this topic faces:

- Design of digital ASICS in nanometer technologies.

- Design of digital cells optimized for several parameters (i.e., dynamic power consumption, leakage, speed, area, noise, ...).

- Timing problems in digital circuits.

- Combined techniques for power and noise reduction in digital circuits.

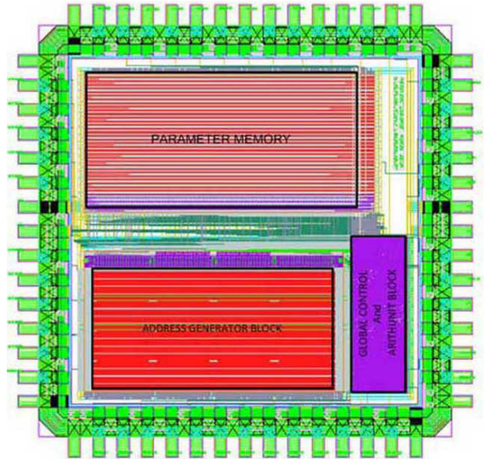
Main results achieved include:
- Design, fabrication and test of digital ASICs following full-custom and semi-custom methodologies, in different technologies, including nanometric ones, for applications in control, security, communication, computational intelligence, etc.

- Development of an automatic and systematic methodology for testing ASICs in the laboratory.

- Design of robust cells and circuits against timing failures, with very low power consumption, low switching-noise generation, and data-independent power consumption.

- Development of different combined noise-power (dynamic and leakage) reduction techniques.

Caption: Test board and ASIC incorporating a double-memory programmable and configurable PWAG controller



Caption: Layout of a 4-input 2-output PWA controller designed in a 90nm technology

Keywords
High-Performance Digital Design; ASICs; Timing Problems; Low-Power and Low-Noise Techniques; Design of Digital Cells

Research Highlights

◆ P. Brox, M.C. Martínez-Rodríguez, E. Tena-Sánchez, I. Baturone and A.J. Acosta, "Application specific integrated circuit solution for multi-input multi-output piecewise-affine functions", International Journal of Circuit Theory and Applications, vol. 44, no. 1, pp. 4-20, 2016

◆ M.C. Martínez-Rodríguez, P. Brox and I. Baturone, "Digital VLSI implementation of piecewise-affine controllers based on lattice approach", IEEE Transactions on Control Systems Technology, vol. 23, no. 3, pp. 842-854, 2015

◆ A.J. Acosta, "Low Power and Security Trade-off in Hardware: From True Random Number Generators to DPA Resilience", Conferencia invitada al Energy Secure Systems Architecture Workshop ISCA 2014, Minnessotta, USA

◆ P. Brox, J. Castro-Ramírez, M.C. Martínez-Rodríguez, E. Tena, C.J. Jiménez, I. Baturone and A.J. Acosta, "A Programmable and Configurable ASIC to Generate Piece-wise-Affine Functions Defined Over General Partitions", IEEE Trans. on Circuits and Systems I: Regular Papers, vol. 60, no. 12, pp. 3182-3194 , 2013
Technology Transfer

◆ A.J. Acosta, I. Baturone, J. Castro-Ramírez, C.J. Jiménez, P. Brox and M.C. Martínez-Rodríguez. Method for generating piecewise-affine multivariable functions with on-line computation of the search tree and device for implementing same. 2012

Key Research Projects & Contracts

INTERVALO: Integration and validation in laboratory of countermeasures against side-channel attacks in microelectronic cryptocircuits (TEC2016-80549-R)
PI: Antonio J. Acosta Jiménez / Carlos J. Jiménez Fernández
Funding Body: Min. de Economía, Industria y Competitividad
Dec 2016 - Dec 2019

CESAR: Secure microelectronic circuits against side-channel attacks (TEC2013-45534-R) » web
PI: Antonio J. Acosta Jiménez / Carlos J. Jiménez Fernández
Funding Body: Min. de Economía y Competitividad
Jan 2014 - Dec 2016

CITIES: Integrated circuits for transmitting secure information (TEC2010-16870) » web
PI: Carlos J. Jiménez Fernández
Funding Body: Min. de Ciencia e Innovación
Jan 2011 - Sep 2014

MOBY-DIC: Model-based synthesis of digital electronic circuits for embedded control (EC-IST-VIIPM no.-248858)
PI: Antonio J. Acosta Jiménez
Funding Body: 7th Framework Programme, European Commission
Dec 2009 - Nov 2013

CRIPTO-BIO: Microelectronic design for crypto-biometric authentication (P08-TIC-03674) » web
PI: Iluminada Baturone Castillo
Funding Body: Junta de Andalucía - Proyectos de Excelencia
Jan 2009 - Dec 2013

Digital Embedded Systems and IoT

Contact

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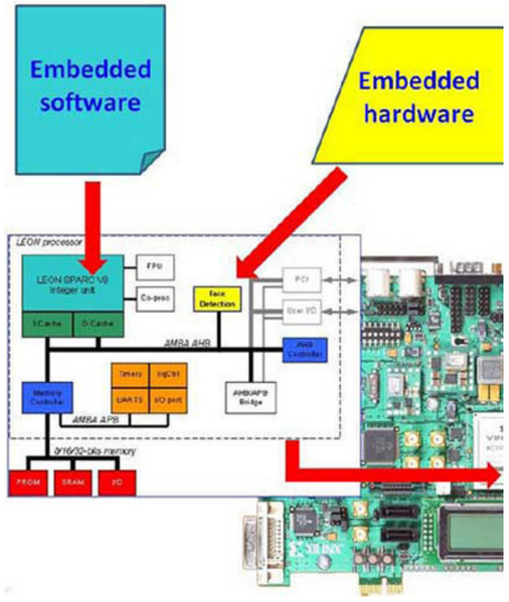
This research line is focused on the design of digital embedded systems implemented on programmable devices (FPGAs), using intellectual property (IP) modules. The aim is to solve problems related to size constraints, power consumption and computation that characterize such systems, as well as to provide the tools and design methodologies that facilitate and accelerate its development. The highlights of the developed solutions are the design of specific processing architectures, hardware/software codesign techniques, the use of reconfigurable devices, and the employment of Intellectual Property (IP) modules for reusability. The transversal nature of this research line allows that its results can be used in different application domains related to other research activities of the group.
The topics of interest that are covered by this research line are:

- Development of design methodologies for embedded digital systems.
  · Specification languages.
  · Hardware & software codesign.
  · CAD tools development.

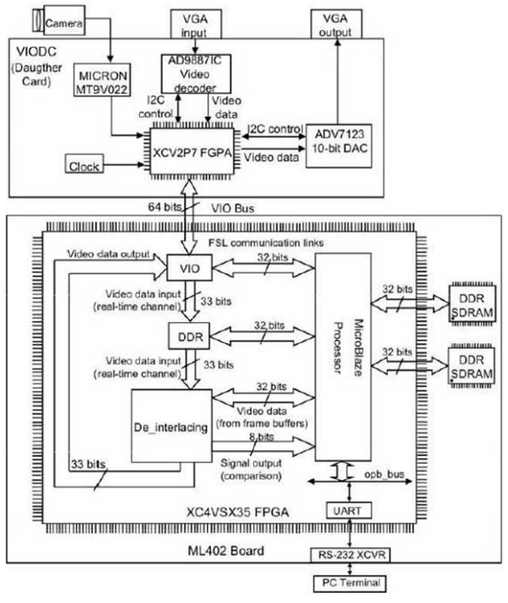
- Architectures for specific application systems.
  · Architectures and design of data/signal processing modules
  · Development of IP modules.
  · Reconfigurable systems

- Applications of embedded digital systems.
  · Biometric systems based on fingerprint, face and voice.
  · Cryptographic systems
  · Image processing and artificial vision
  · Emerging applications of wearables, smart cards, communications networks, industrial control systems, wireless sensor networks and Internet of Things.

Keywords
Embedded Systems; Design Methodologies; Systems



Caption: FPGA-Based Embedded System to Implement Viola-Jones Face Detection Algorithm



Caption: FPGA-Based Embedded System for Video De-Interlacing. a) Block Diagram. b) Experimental Setup

on Chip (SoC); Hardware & Software Codesign; Reconfigurable Devices; CAD Tools

Research Highlights

◆ M.J. Avedillo, A. Barriga, L. Acasandrei and J.M. Calahorro, "Hardware-software embedded face recognition system", International Conferences in Central Europe on Computer Graphics, Visualization and Computer Vision (WSCG), Pilzen, Czech Republic, 2016

◆ E. Calvo-Gallego, P. Brox and S. Sanchez-Solano, "Low-cost dedicated hardware IP modules for background subtraction in embedded vision systems", Journal of Real-Time Image Processing, vol. 12, no. 4, pp. 681-695, 2016

◆ P. Brox, I. Baturone and S. Sánchez-Solano, "Fuzzy logic-based embedded system for video de-interlacing", Applied Soft Computing, vol. 14, part C, pp. 338-346, 2014

◆ M. Brox, S. Sánchez-Solano, E. del Toro, P. Brox and F.J. Moreno-Velo, "CAD tools for hardware implementation of embedded fuzzy systems on FPGAs", IEEE Transactions on Industrial Informatics, Special Section on Embedded and Reconfigurable Systems, vol. 9, no. 3, pp. 1635-1644, 2013

Key Research Projects & Contracts

ID-EO: Design of crypto-biometric hardware for video encryption and authentication (TEC2014-57971-R)
PI: Iluminada Baturone Castillo / Piedad Brox Jiménez
Funding Body: Min. de Economía y Competitividad
Jan 2015 - Dec 2018

SENIAC: Security in interconnected devices by injection of authentication and ciphering algorithms (RTC-2014-2932-8)
PI: Iluminada Baturone Castillo
Funding Body: Min. de Economía y Competitividad
Oct 2014 - Mar 2017

SEIs: Hardware design for embedded systems in intelligent environments (TEC2011-24319)
PI: Santiago Sánchez Solano
Funding Body: Min. de Ciencia e Innovación
Jan 2012 - Sep 2015

MOBY-DIC: Model-based synthesis of digital electronic circuits for embedded control (EC-IST-VIIPM no.-248858)
PI: Antonio J. Acosta Jiménez
Funding Body: 7th Framework Programme, European Commission
Dec 2009 - Nov 2013

CRIPTO-BIO: Microelectronic design for crypto-biometric authentication (P08-TIC-03674)
PI: Iluminada Baturone Castillo
Funding Body: Junta de Andalucía - Proyectos de Excelencia
Jan 2009 - Dec 2013

RESEARCH AREA ◆ BRAIN-INSPIRED NEURAL NETWORKS AND ARTIFICIAL INTELLIGENCE

Neuromorphic Cognitive Systems

Contact

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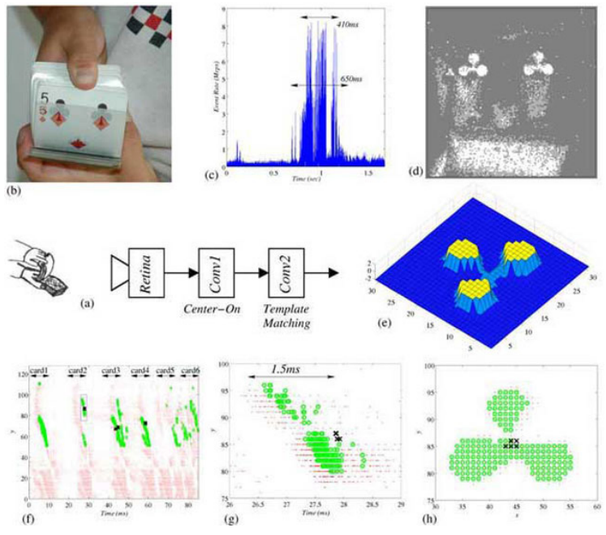
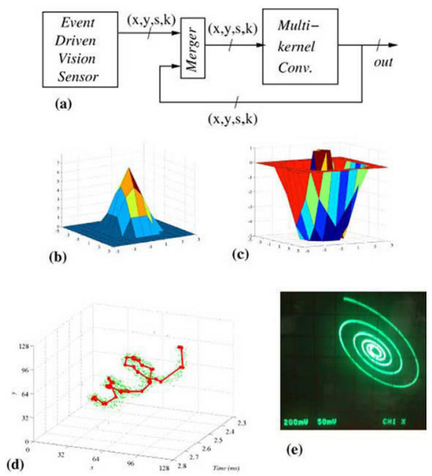
The IMSE Neuromorphic group develops sensory and processing microchips that mimic sensing and processing in biological beings. It also develops multi-chip and hybrid chip-FPGA systems to scale up to higher complexity systems. The group also works on algorithms and sensory processing for spiking information sensing, coding and processing. Chips use mixed signal, low current, and/or low power, circuit techniques, as well as high speed communication techniques. The group uses mixed or digital CMOS technologies, as well as application projections exploiting emergent nanoscale technologies or new devices like memristors.
At present, the group focuses mainly on event-driven (spiking) frame-free vision systems, developing sensing retinas for spatial or temporal contrast (such as DVS -Dynamic Vision Sensors), as well as event-driven convolution processors, which allow to assemble for example large scale spiking 'Convolutional Neural Networks' for high speed object recognition. These chips and systems use AER (Address Event Representation) communication techniques.
Event-driven retinas do not produce sequences of still frames, as conventional video cameras do. Instead, each pixel senses light and computes a given property (spatial contrast, temporal change) continuously in time. Whenever this property exceeds a given threshold, the pixel sends out an event (which usually consists of the pixel x,y coordinate and the sign of the threshold), which is written onto one (or more) high speed bus with asynchronous handshaking. This way, sensors produce continuous event flows, and subsequent processors process them event by event.

Keywords
Spiking Neural-Circuits; Signal-Processing; Learning; AER (Address-Event-Representation); AER-Contrast-Retinas; AER Dynamic Vision Sensors (DVS); Memristive Neuromorphic Systems; AER-Processors; AER-Convolution; STDP (Spike-Timing-Depen-



Caption: Event-driven shape sensing-recognition. (a) system, (b) stimulus, (c) events, (d-f) stages outputs showing 'clover' recognition simultaneous to stimulus. See ref [B] for details.



Caption: Event-driven sensing-processing system with (a) DVS-retina and multi-kernel-convolver (b,c): it captures the 500Hz oscilloscope spiral (e), generating events (x,y,t), representing the spatio-temporal trajectory (d). See ref [A] for details.

dent-Plasticity); Low-Power; Frame-Free-Vision; Convolutional-Neural-Networks

Research Highlights

◆ A. Yousefzadeh, M. Khoei, S. Hosseini, P. Holanda, S. Leroux, O. Moreira, J. Thapson, B. Dhoet, P. Simoens, T. Serrano-Gotarredona, and B. Linares-Barranco, "Asynchronous Spiking Neurons, the natural key to exploit temporal sparsity", IEEE Journal on Emergent and Selected Topics in Circuits and Systems, vol. 9, no. 4, pp. 668-678, 2019

◆ A. Yousefzadeh, E. Stromatias, M. Soto, T. Serrano-Gotarredona and B. Linares-Barranco, "On Practical Issues for Stochastic STDP Hardware with 1-bit Synaptic Weights", Frontiers in Neuroscience, vol. 12, article 665, 2018

◆ A. Yousefzadeh, M. Jablonski, T. Iakymchuk, A. Linares-Barranco, A. Rosado, L.A. Plana, S. Temple, T. Serrano-Gotarredona, S. Furber, and B. Linares-Barranco, "On Multiple AER Handshaking channels over High-Speed Bit-Serial Bi-Directional LVDS Links with Flow-Control and Clock-Correction on Commercial FPGAs for Scalable Neurmorphic Systems", IEEE Trans. on Biomedical Circuits and Systems, vol 11, no. 5, pp. 1133-1147, 2017

◆ [B] J. A. Pérez-Carrasco, B. Zhao, C. Serrano, B. Acha, T. Serrano-Gotarredona, S. Chen and B. Linares-Barranco, "Mapping from Frame-Driven to Frame-Free Event-Driven Vision Systems by Low-Rate Rate-Coding and Coincidence Processing. Application to Feed-Forward ConvNets," IEEE Trans. on Pattern Analysis and Machine Intelligence, vol. 35, no. 11, pp. 2706-2719, 2013

◆ [A] L. Camuñas-Mesa, C. Zamarreño-Ramos, A. Linares-Barranco, A. Acosta-Jiménez, T. Serrano-Gotarredona and B. Linares-Barranco, "An Event-Driven Multi-Kernel Convolution Processor Module for Event-Driven Vision Sensors," IEEE Journal of Solid-State Circuits, vol. 47, no. 2, pp. 504-517, 2012

Technology Transfer
Spin-off Company: Prophesee. Metavision for machines
Spin-off Company: GrAI Matter Labs. Create magic on the edge with GrAI One

Key Research Projects & Contracts

SPINAGE: Weighted Spintronic-Nano-Oscillator-based Neuromorphic Computing System Assisted by laser for Cognitive Computing
PI: Teresa Serrano-Gotarredona
Funding Body: European Union
Oct 2020 - Sep 2024

NeurONN: Two-Dimensional Oscillatory Neural Networks for Energy Efficient Neuromorphic Computing
PI: Bernabé Linares-Barranco
Funding Body: European Union
Jan 2020 - Dec 2022

HBP: Human Brain Project
PI: Bernabé Linares-Barranco
Funding Body: European Union
Apr 2014 - Mar 2016

NABAB: Nanocomputing Building Blocks with Acquired Behaviour
PI: Teresa Serrano Gotarredona
Funding Body: European Union
Apr 2007 - Apr 2010

CAVIAR: Convolution AER Vision Architecture
PI: Bernabé Linares-Barranco
Funding Body: European Union
Jun 2002 - Jun 2006s

Microelectronic Systems for Computational Intelligence

Contact

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This research line focuses on the development of new design methodologies and circuit elements for Computational Intelligence applications. Computational Intelligence includes a set of techniques inspired by natural processes that allow addressing complex problems more efficiently than through traditional approaches. Specifically, our interest is mainly focused towards efficient hardware implementation of neuro-fuzzy systems and its use in applications that take advantage of their ability to describe a system with linguistic terms, as well as to cope with the inaccurate, vague or incomplete information that appears in many real-world problems.
In recent years, the developed activities in this line have addressed the following three main objectives:
- The development of architectures for efficient implementation of fuzzy-inference systems on ASICs and FPGAs, as well as the proposal of a model-based design methodology that accelerates the stages of functional verification and synthesis of fuzzy modules and facilitates their integration in embedded systems.

- The generation of a development environment for fuzzy systems, Xfuzzy, which facilitates the tasks of design, verification and synthesis, both software and hardware, of fuzzy logic-based systems.

- The application of the above techniques and circuits to different problems of robotics, industrial control, food technology, communications systems, image processing, and intelligent device networks for applications related to the areas of safety and environmental control.

Keywords
Intelligent Systems; Soft-Computing; Neuro-Fuzzy Circuits; CAD Tools; Model-Based Design; Fuzzy Control; Fuzzy Image Processing; Internet of Things

Research Highlights

◆ S. Sánchez-Solano and M. Brox, "Hardware Implementation of Embedded Fuzzy Controllers on FPGAs and ASICs", in Fuzzy Modelling and Control: Theory and Applications, vol. 9, pp. 235-253, Atlantis Series on Computational Intelligence Systems, Springer-Verlag, 2014

◆ S. Sánchez-Solano, E. del Toro, M. Brox, P. Brox and I. Baturone, "Model-Based Design Methodology for Rapid Development of Fuzzy Controllers on FPGAs", IEEE Trans. on Industrial Informatics, vol. 9, no. 3, pp. 1361-1370, 2013

◆ P. Brox, I. Baturone and S. Sánchez-Solano, "Fuzzy Logic-Based Algorithms for Video De-Interlacing", Series: Studies in Fuzziness and Soft Computing, vol. 246, Springer, 2010

◆ S. Sánchez-Solano, A. J. Cabrera, I. Baturone, F.J. Moreno-Velo and M. Brox, "FPGA Implementation of Embedded Fuzzy Controllers for Robotic Applications", IEEE Trans. on Industrial Electronics, vol. 54, no. 4, pp. 1937-1945, 2007

◆ I. Baturone, A. Barriga, S. Sánchez-Solano, C.J. Jiménez-Fernández and D.R. López, Microelectronic Design of Fuzzy Logic-Based Systems, CRC Press, 2000

Key Research Projects & Contracts

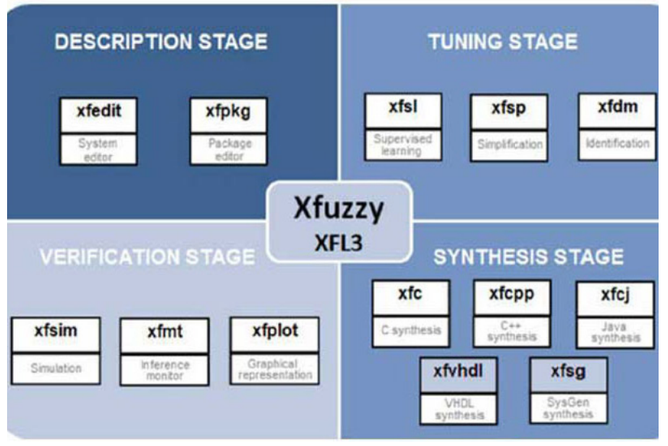
Predicción regional de potencia eólica a partir de Lógica Difusa
PI: Iluminada Baturone Castillo
Funding Body: EDP Renováveis
2014 - 2015

SEIs: Diseño hardware para sistemas empotrados en entornos inteligentes (TEC2011-24319)
PI: Santiago Sánchez Solano
Funding Body: Min. de Ciencia e Innovación
Jan 2012 - Sep 2015

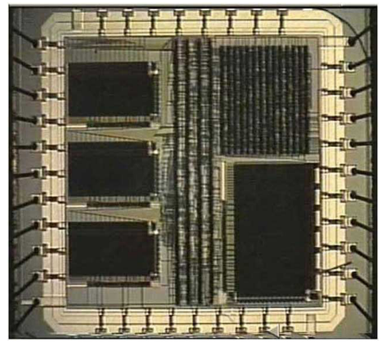
DIMISION: Diseño microelectrónico de sistemas de visión para redes de sensores inteligentes (TEC2008-04920)
PI: Santiago Sánchez Solano
Funding Body: Min. de Ciencia e Innovación
Jan 2009 - Jun 2012

FVISION: Implementación microelectrónica de circuitos difusos para microsistemas inteligentes de visión (TEC2005-04359/MIC)
PI: Ángel Barriga Barros
Funding Body: Min. de Ciencia y Educación
Dec 2005 - Dec 2008

Diseño microelectrónico de sistemas inteligentes para el procesado de información sensorial (TIC2001-1726-C02-01)
PI: Santiago Sánchez Solano
Funding Body: Gobierno de España
2001-2004



Caption: VLSI implementation of a 3-input 1-output fuzzy inference system using an active rule-based architecture.



Caption: Components of the Xfuzzy environment, which integrates tools to facilitate the different stages involved in the design process of fuzzy logic-based systems.

RESEARCH AREA ◆ SENSORY & PHOTONIC VISION SYSTEMS

CMOS Smart Imagers and Vision Chips

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Image handling is instrumental in many applications, including consumer electronics, surveillance, robotics, machine vision, etc. Some of them demand high quality images, while others require fast analysis and interpretation of the image flow. Despite the specific target, all applications benefit from embedding processing circuitry together with optical sensors in the same silicon substrate. CMOS technologies allow the incorporation of digital processing on-chip to correct image artifacts or to analyze and interpret the scene in real-time. Using CMOS technologies enables the implementation of cameras and vision systems with reduced power consumption and reduced size. This permits the incorporation of vision in applications where it was previously considered to be economically prohibitive or technically unfeasible.
This research line embraces different activities related to the incorporation of intelligence into image sensors, namely:
- New pixel topologies for enhanced sensitivity and reduced noise.

- Front-side and Back-side illuminated sensors.

- Pixels for single-photon detection and time-of-flight calculations.

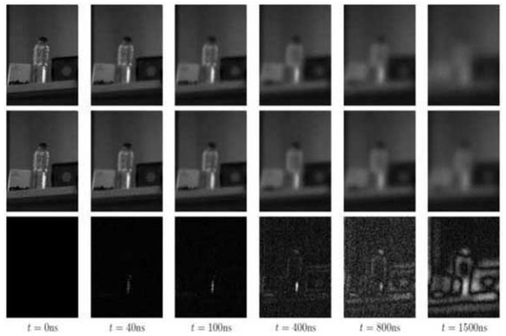
- Pixels for high-dynamic range image acquisition.

- In-pixel processing and memory for feature extraction at the focal-plane.

- Re-configurable read-out channels for high-performance digital imagers.

- Data converters for high-speed and high accuracy (low noise) image downloading.

- Architectures and algorithms for on-chip image correction.



Caption: On-chip generated scale-space (upper row) compared to ideal (middle row). Gaussian filters are implemented by time-controlled diffusion.

- Distributed, progressive processing architectures for vision systems.

- Sensors for 3-D image capture.

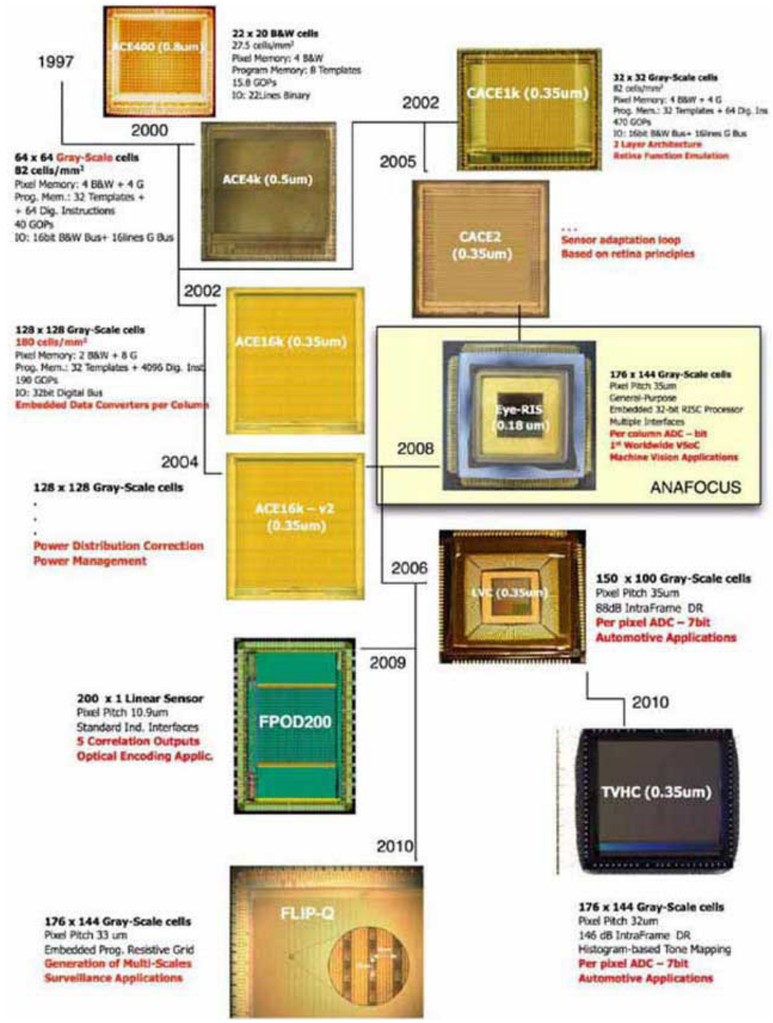
Different application areas are covered like automotive, unmanned vehicle navigation, distributed smart cameras and vision-enabled wireless sensor networks. These applications have been benchmarked by using real systems. Significant parts of the technology have been transferred to industry, including the creation of spin-off companies.

Keywords
Smart CMOS Imagers; HDR Imagers; Real-Time Vision Systems-on-Chip; Data Converters for Imagers; Silicon Retinas

Research Highlights

◆ J. Fernandez-Berni, R. Carmona-Galan and A. Rodriguez-Vazquez, Low-Power Smart Imagers for Vision-Enabled Sensor Networks, Springer, 2012

◆ J. Fernandez-Berni, R. Carmona-Galan and L. Carranza-Gonzalez. "FLIP-Q: A QCIF Resolution Focal-Plane Array for Low-Power Image Processing", IEEE Journal of Solid-State Circuits, vol. 46, no. 3, pp. 669-680, 2011
G. Liñan, A. Rodriguez-Vazquez, R. Carmona, F. Jimenez, S. Espejo and R. Dominguez-Castro, "A 1000 FPS@128x128 Vision Processor with 8-bit Digitized I/O", IEEE Journal of Solid-State Circuits, vol 39, no. 7, pp. 1044-1055, 2004



Caption: Chronology of the vision chips designed by the group, from 1997 to 2010

◆ A. Rodriguez-Vazquez, G. Liñan, L. Carranza, E. Roca, R. Carmona, F. Jimenez-Garrido, and R. Dominguez-Castro, "ACE16k: the Third Generation of Mixed-Signal SIMD-CNN ACE Chips towards VSoCs", IEEE Transactions on Circuit and Systems I: Fundamental Theory and Applications, vol. 51, no. 5, pp. 851-863, 2004

◆ T. Roska and A. Rodriguez-Vazquez (Eds.), Towards the Visual Microprocessor: VLSI Design and the Use of Cellular Neural Network Universal Machine Computers, pp. 213-237, John Wiley & Sons, 2001

Key Research Projects & Contracts

3DHVC: Design of high-performance heterogeneous, ultra high speed cellular sensor-processors for multispectral light sensing (BAA-11-001)
PI: Ángel Rodríguez Vázquez
Funding Body: Office of Naval Research (USA)
Jan 2011 - Dec 2013

WIVISNET: Wireless and smart vision sensors for networked surveillance and monitoring (TEC2009-11812)
PI: Ricardo Carmona Galán
Funding Body: Min. de Ciencia e Innovación
Jan 2010 - Dec 2012

VISTA: Design of sensing-processing-actuation systems on-a-chip: 4th generation vision systems (TIC2003-09817-C02-C01)
PI: Ángel Rodríguez Vázquez
Funding Body: Min. de Ciencia y Tecnología
Dec 2003 - Nov 2006

Heterogeneous Sensory-Processing Systems and 3-D Integration

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3D Integration technologies enable vertical interconnection of different wafers and thus the allocation of different subsystems and functions into dedicated, specialized layers. Both features have significant impact on performance. On the one hand, different technologies and materials can be combined, for instance nano-antennas for THz radiation detectors. On the other hand, form factors can be improved and larger function densities can be achieved; for instance, image pixels with embedded processing can be effectively implemented without penalizing the fill factor and the pixel pitch.
This research comprises different activities concerning heterogeneous sensory-processing systems using 3D IC with emphasis on technologies employing TSVs.
Activities include the following:
- Prospective analysis and identification of suitable 3D technology candidates.

- Multi-spectral, 3D-compatible sensing materials and devices.

- Interface circuitry between these sensors and the processing layers, including the electrical interface itself as well as the time multiplexing which may be required to handle different signal granularities at the different layers.

- Architectures for optimum exploitation of the potentials of 3D heterogeneous technologies. Emphasis is on vision systems and the usage of different spatial resolutions and scales at each layer in the vertically-interconnected architecture.

- Identification of constitutive functional operators for the different layers of the vertical processing chain, with emphasis on vision.

- Circuit topologies for the different layers of the processing chain.

Regarding vision systems, the basic challenge is to achieve sensors with million pixel counts, pixel pitch around 6μm and operating speed in the range of 10,000 Frames/second.

Keywords
3D Integrated Circuits; Through-Silicon-Vias; Vertically-Interconnected Systems; Heterogeneous Integration

Research Highlights

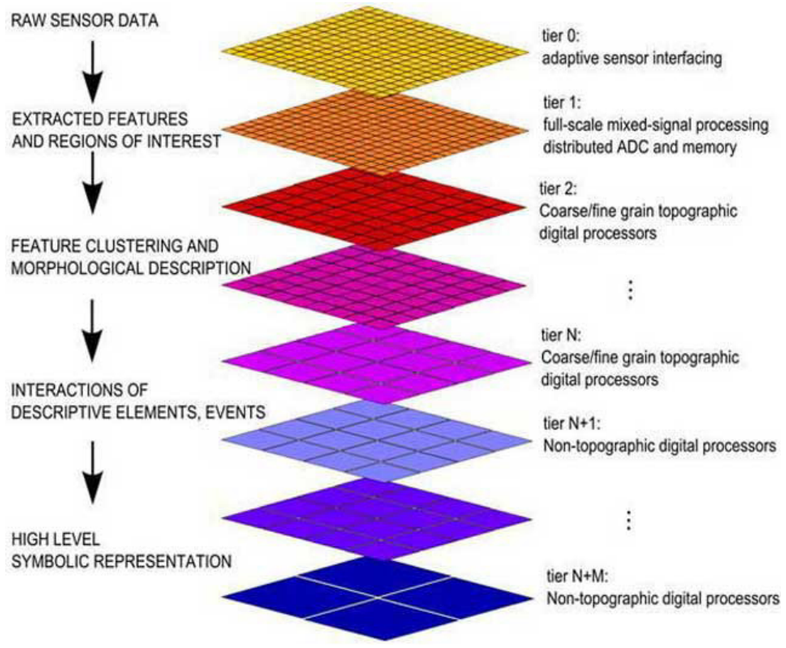
◆ R. Carmona-Galan, A. Zarandy, Cs. Rekeczky, P. Földesy, A. Rodriguez-Perez, C. Dominguez-Matas, J. Fernandez-Berni, G. Liñan-Cembrano, B. Perez-Verdu, Z. Karasz, M. Suarez-Cambre, V. M. Brea-Sanchez, T. Roska and A. Rodriguez-Vazquez, "A hierarchical vision processing architecture oriented to 3D integration of smart camera chips", Journal of Systems Architecture, vol. 69, no. 10, part A, pp. 908-919, 2013

◆ M. Suarez, V.M. Brea, J. Fernandez-Berni, R. Carmona-Galan, G. Liñan, D. Cabello and A. Rodriguez-Vazquez, "CMOS-3D Smart Imager Architectures for Feature Detection", IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 2, no. 4, pp. 723-736, 2012

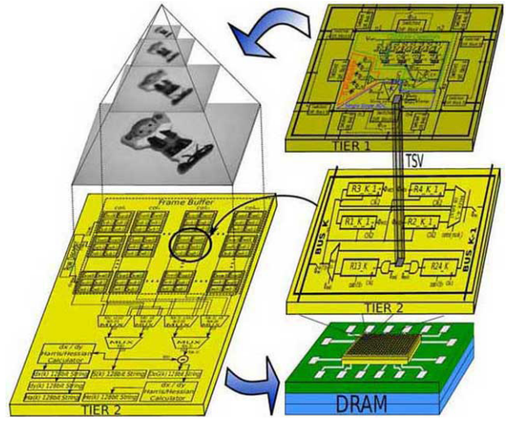
◆ A. Zarandy, Cs. Rekeczky, P. Földesy, R. Carmona-Galan, G. Liñan-Cembrano, G. Sos, A. Rodriguez-Vazquez and T. Roska, "VISCUBE: a multi-layer vision chip", in Á. Zarandy (Ed.), Focal-Plane Sensor-Processor Chips, pp. 181-208, Springer, 2011

◆ A. Zarandy, P. Földesy, R. Carmona-Galan, Cs. Rekeczky, J. Bean and W. Porod, "Cellular Multi-core Processor Carrier Chip for Nanoantenna Integration and Experiments", in Ch. Baatar, W. Porod & T. Roska (Eds.), Cellular Nanoscale Sensory Wave Computing, , pp. 147-168, Springer, 2010

◆ R. Maldonado-Lopez, F. Vidal-Verdu, G. Liñan and A. Rodriguez-Vazquez, "Integrated Circuitry to Detect Slippage Inspired by Human Skin and Artificial Retinas", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 56, no. 8, pp. 1554-1565, 2009



Caption: Functional/ physical mapping in a multilayer structure



Caption: A CMOS-3D reconfigurable architecture with In-pixel processing for feature detectors

Key Research Projects & Contracts

INNPACTO 3D2: Intelligent Image Sensors in CMOS Technology with 3D Stacked Chips (IPT-2011-1625-430000)
PI: Ángel Rodríguez Vázquez
Funding Body: Min. de Ciencia e Innovación
May 2011 - Dec 2014

3DHVC: Design of high-performance heterogeneous, ultra high speed cellular sensor-processors for multispectral light sensing (BAA-11-001)
PI: Ángel Rodríguez Vázquez
Funding Body: Office of Naval Research, USA
Jan 2011 - Dec 2013

Study and design of interfaces for CMOS-compatible sensing nanostructures for the integration of nanoelectronic systems
PI: Ricardo Carmona Galán
Funding Body: Min. de Educación y Ciencia
Oct 2006 - Sep 2007

Dynamic Vision Sensors

Contact

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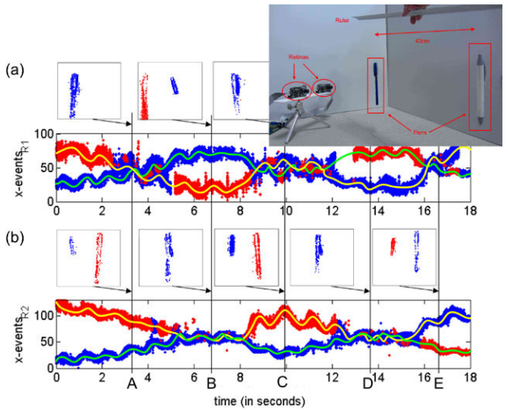
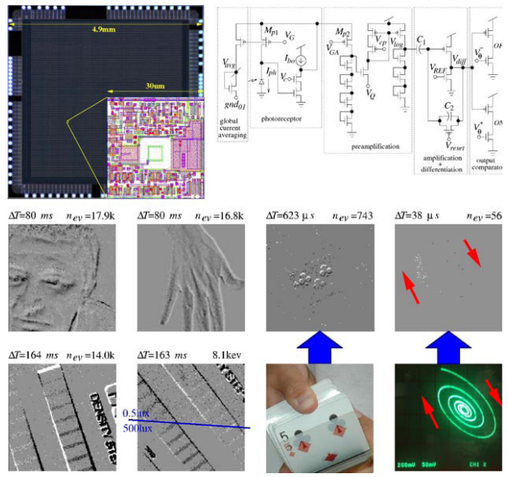
Dynamic Vision Sensors are a type of spiking silicon retinas in which each pixel autonomously and asynchronously sends out an address event when the light it senses has changed above a given relative threshold. This type of cameras, which are "Frame-Free", do not generate sequences of still frames, as conventional commercial cameras do, but provide a flow of spiking address events that dynamically represent the changing visual scene. They are heavily inspired in biological retinas, which also send continuously nervous spike impulses to the cortex. Biological retinas are continuously vibrating through microsaccades and ocular tremors, thus producing spikes also when there is change of light. DVS cameras provide an almost instantaneous representation (with micro-second delays) of the changing visual reality, with very reduced data flow, reduced power, and data sparsity, thus reducing data processing requirements of subsequent stages. DVS cameras have become of high interest to industry recently with a number of spinoff companies commercializing them (Prophesee, IniVation, Celepixel as well as large traditional companies like Samsung and Sony embracing developments.
At IMSE there is a specific research line on AER (Address Event Representation) DVS cameras by the Neuromor-



Caption: 3D Stereo Vision with a pair of DVS cameras solving correct object tracking with temporal occlusions. See ref [B] for details.



Caption: Top: DVS chip with 128x128 pixels, showing zoom preview of 30µm size pixel and schematic on the right, fabricated in AMS 0.35µm. Bottom: Example captures of DVS camera showing high-speed capability, low data-rate (nev is number of events), high intra-scene dynamic range. See ref [A] for details.

phic Group, who coordinated the CAVIAR EU project in which this type of sensor was first invented and exploited. Later on they developed their own prototype which at that time had the best contrast sensitivity, power consumption, and circuit compactness, resulting in 4 licensed patents and the participation in French spin-off company Chronocam, now known as Prophesee.
Main recent activities in this line include:

- Design and fabrication of a number of Dynamic Vision Sensors.

- Improved AER read-out circuitry.

- Design of improved temporal contrast sensitivity prototypes through low power mismatch-insensitive amplification stages.

- Development of new conceptual circuits for alternative operation principles for DVS cameras.

- Low current circuit techniques.

- Fast read-out circuits.

Keywords
Dynamic Vision Sensor; Address Event Representation; Spiking Retinas; Spiking Neural Networks; Asynchronous Circuits; High-Speed Low-Power Vision; DVS Stereo-Vision

Research Highlights

◆ A. Yousefzadeh, G. Orchard, T. Serrano-Gotarredona and B. Linares-Barranco, "Active Perception with Dynamic Vision Sensors. Minimum Saccades with Optimum Recognition", IEEE Transactions on Biomedical Circuits and Systems, vol. 12, no. 4, pp 927-939, 2018

◆ [B] L.A. Camuñas-Mesa, T. Serrano-Gotarredona, S. Ieng, R. Benosman and B. Linares-Barranco, "Event-Driven Stereo Visual Tracking Algorithm to Solve Object Occlusion", IEEE Transactions on Neural Networks and Learning Systems, vol. 29, no. 9, pp 4223-4237, 2017
T. Serrano-Gotarredona and B. Linares-Barranco, "Poker-DVS and MNIST-DVS. Their History, How They were Made, and Other Details", Frontiers in Neuromorphic Engineering, Frontiers in Neuroscience, vol. 9, article 481, 2015

◆ [A] T. Serrano-Gotarredona and B. Linares-Barranco, "A 128x128 1.5% Contrast Sensitivity 0.9% FPN 3µs Latency 4mW Asynchronous Frame-Free Dynamic Vision Sensor Using Transimpedance Amplifiers", IEEE Journal of Solid-State Circuits, vol. 48, no. 3, pp 827-838, 2013

◆ J.A. Leñero-Bardallo, T. Serrano-Gotarredona and B. Linares-Barranco, "A 3.6µs Latency Asynchronous Frame-Free Event-Driven Dynamic-Vision-Sensor", IEEE Journal of Solid-State Circuits, vol. 46, no. 6, pp 1443-1455, 2011

◆ Technology Transfer
Patent: T. Finateu, B. Linares-Barranco, C. Posch and T. Serrano-Gotarredona, "Pixel Circuit for Detecting Time-Dependent Visual Data", WO2018073379A1. Priority 20-Oct-2016. European patent, extended to US, Korea, Japan, China.

◆ Patent: T. Finateu, B. Linares-Barranco, C. Posch and T. Serrano-Gotarredona, "Sample and Hold based Temporal Contrast Vision Sensor", WO2017174579A1. Priority: 4-Apr-2016.

◆ Patent: B. Linares-Barranco and T. Serrano-Gotarredona, "Method and Device for Detecting the Temporal Variation of the Light Intensity in a Matrix of Photosensors", WO2014091040A1. Priority: 11-Dec-2012. European patent, extended to US, Korea, Japan, Israel.

◆ Patent: B. Linares-Barranco and T. Serrano-Gotarredona, "Low-Mismatch and Low-Consumption Transimpedance Gain Circuit for Temporally Differentiating Phot-Sensing systems in dynamic vision Sensors", WO2012160230A1. Priority: 26-May-2011. European patent, extended to US, Korea, Japan, China.

◆ Spin-off Company: Prophesee. Metavision for machines.

Key Research Projects & Contracts

APROVIS3D: Analog PROcessing Of Bioinspired Vision Sensors For 3D Reconstruction
PI: Teresa Serrano Gotarredona
Funding Body: Min. de Ciencia e Innovación
Apr 2020 - March 2023

COGNET: Event-based cognitive vision system. Extension to audio with sensory fusion
PI: Teresa Serrano Gotarredona
Funding Body: Min. de Ciencia e Innovación
Jan 2016 - Dec 2019

ECOMODE: Event-driven compressive vision for multimodal interaction with mobile devices
PI: Bernabé Linares-Barranco
Funding Body: European Union
Jan 2015 - Dec 2018

BIOSENSE: Bioinspired event-based system for sensory fusion and neurocortical processing. High-speed low-cost applications in robotics and automotion.
PI: Teresa Serrano Gotarredona
Funding Body: Min. de Ciencia e Innovación
Jan 2013 - Dec 2015

NANONEURO: Design of neurocortical architectures for vision applications
PI: Teresa Serrano Gotarredona
Funding Body: Junta de Andalucía
Jul 2011 - Dec 2014

RESEARCH AREA ◆ NANOELECTRONICS AND EMERGING TECHNOLOGIES

Circuit Design using Emerging Devices and Non-Conventional Logic Concepts

Contact

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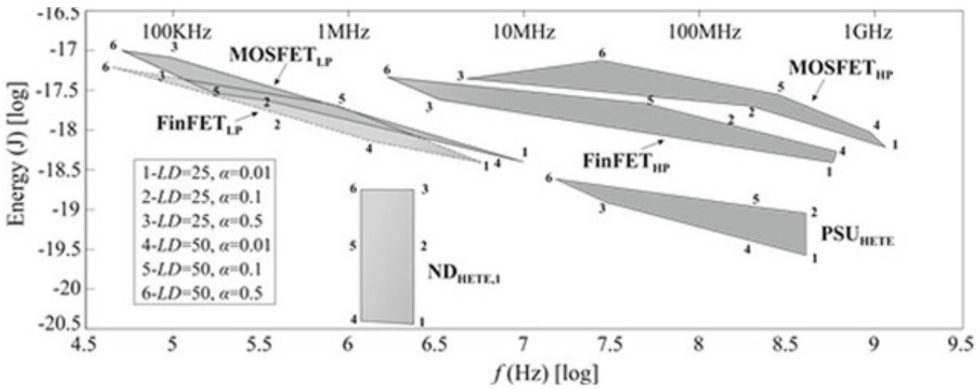
Main research objective is the development, analysis and design of circuits using emerging devices and/or nonconventional logic models, with emphasis on applications with severe constraints on power or energy like IoT. In particular, we explore circuits based on resonant tunel diodes (RTDs), tunel transistors (TFETs and SymFETs) or devices integrating phase transition (Hyper-FETs, VO2). The distinguishing features of these devices is exploited to obtain circuits competitive with respect to their CMOS counterparts in terms of speed, power, energy or area or exhibiting better trade-offs among those criteria. From the logic point of view, we study threshold logic and more recently oscillator-based computing.
Main recent activities in this line include:
- Development of oscillatory neural networks in which the synchronization dynamics of oscillators are used for computation. Oscillators are implemented with a VO2 device and a transistor.

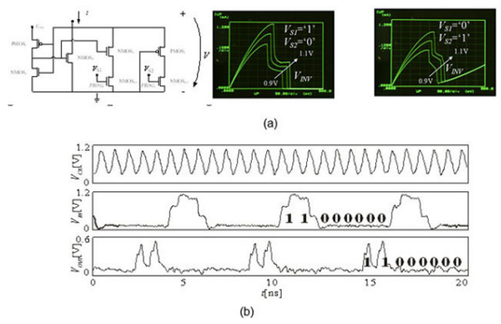
- Development of logic based on the coding of information in the phase of an oscillation. Its main element is an oscillator to which a synchronization signal is injected to discretize its phase. In the case of binary logic, only two phases are used.

- Design and evaluation of logic circuits using TFETs and HyperFETs for low power and energy efficient applications. Technology benchmarlking and identification of application areas, development of gate topologies and logic architectures suitable for the specific characteristics of these devices.

Keywords
Emerging Devices; Coupled Oscillators; Oscillatory



Caption: Evaluation in terms of energy and speed of CMOS transistors (MOSFETs and FinFETs) and tunel transistors (PSUHETE and NDHETE1). Different logic-deths and switching activities are explored.



Caption: a) Programable MOS-NDR exhibiting negative differential resistance; b) Experimental results of a two-phase single-gate-per phase MOBILE pipeline.

Neural Networks; Oscillator-based Computing; VO2; Energy Efficiency; Ultra-Low Power Electronic; Resonant Tunel Diode (RTD); Negative Differential Resistance (NDR); Tunel Transistor (TFET); Steep Subthreshold Slope Devices

Research Highlights

◆ M.J. Avedillo, J.M. Quintana and J. Núñez, "Phase Transition Device for Phase Storing", IEEE Transactions on Nanotechnology, vol. 19, pp 107-112, 2020

◆ M. Jiménez, J. Núñez and M.J. Avedillo, "Hybrid Phase Transition FET Devices for Logic Computation", IEEE Journal on Exploratory Solid-State Computational Devices and Circuits, vol. 6, no. 1, pp 1-8, 2020

◆ J. Núñez and J.M. Avedillo, "Approaching the Design of Energy Recovery Logic Circuits using Tunnel Transistors", IEEE Transactions on Nanotechnology, vol. 19, pp 500-507, 2020

◆ J. Núñez and M.J. Avedillo, "Power and Speed Evaluation of Hyper-FET Circuits", IEEE Access, vol. 7, pp 6724-6732, 2019

◆ J. Nuñez and M.J. Avedillo, "Reducing the Impact of Reverse Currents in Tunnel FET Rectifiers for Energy Harvesting Applications", IEEE Journal of the Electron Devices Society, vol. 5, no. 6, pp. 530-534, 2017

Key Research Projects & Contracts

NEURONN: Two-Dimensional Oscillatory Neural Networks for Energy Efficent Neuromorphic computing (H2020-871501)
PI: Bernabé Linares Barranco
Funding Body: European Union
Jan 2020 - Dec 2022

PULPOSS: Processing for Ultra Low POwer using Steep Slope devices: circuits and arquitectures (TEC2017-87052-P)
PI: María J. Avedillo de Juan / José M. Quintana Toledo
Funding Body: Min. de Economía y Competitividad
Jan 2018 - Dec 2020

NACLUDE: Nano-architectures for logic computing using emergent devices (TEC2013-40670-P)
PI: Jose M. Quintana Toledo / María J. Avedillo de Juan
Funding Body: Min. de Economía y Competitividad
Jan 2014 - Dec 2017

RTDs: Architectures and circuits for logic and non-linear applications using RTDs (TEC2010-18937)
PI: María J. Avedillo de Juan
Funding Body: Min. de Ciencia e Innovación
Jan 2011 - Dec 2014

QUDOS: Quantum Tunneling Device Technology on Silicon (IST-2001-32358)
PI: Werner Prost / WP Coordinator: José M. Quintana Toledo
Funding Body: European Comission
Jan 2002 - Dec 2004

Nanoscale Memristor Circuits and Systems

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With the end of Moore's Law approaching quickly, mainstream CMOS downscaling is slowing down. Novel nanoscale emerging devices compatible with CMOS fabrication technologies promise to overcome this slow down. Ultra-dense multi-layer fabrics of nano-scale devices can be fabricated as BEOL (back end of line) on top of CMOS substrates. One of these emerging devices are memristors, also called resistive-RAM (RRAM), which are two-terminal devices whose resistance can be changed as the devices are stimulated differently. Some of these memristors allow for two-state resistances, while other less developed may allow for continuous non-volatile analog memory states. In this research line our main focus is to exploit these novel memristive devices combined with optimized CMOS circuits to provide ultra-compact ultra-low-power computing architectures for edge and IoT applications. Main recent activities in this line include:
- Design and fabrication of monolithic CMOS/memristor Proof-of-Concept computing systems using TiO RRAM Filamentary Memristors.

- Computation of Spike-Time-Dependent-Plasticity Learning Rules with Memristors.

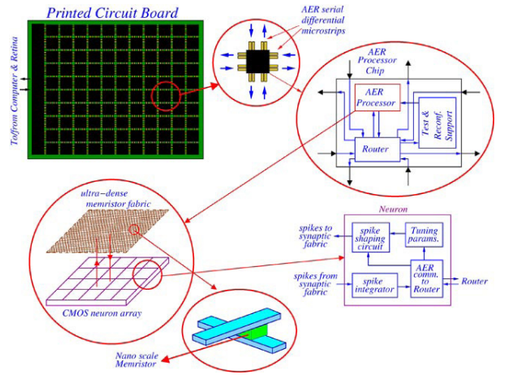
- Stochastic Binary Spike-Time-Dependent-Plasticity for Memristor-based 1-bit weight learning and inference.

- Calibration Techniques for ultra-low-voltage memristive read-out circuits.

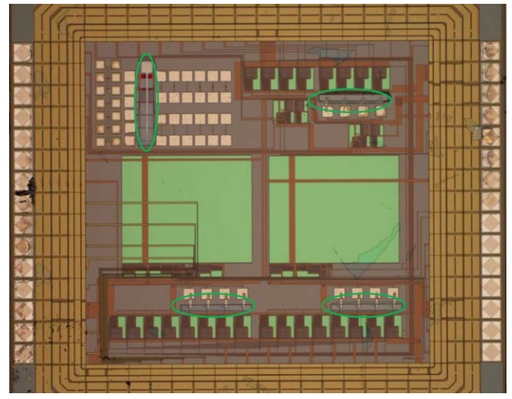
Keywords
RRAM (Resistive RAM); Non-volatile memristor memory; Nanoscale memristors; TiO filamentary memristors; 1T1R memristor crossbars; Spiking neuromorphic computing with memristors; Hopfield Neural Networks with memristors; Spike-Timing-Dependent-Plasticity with memristors

Research Highlights

◆ L. A. Camuñas-Mesa, B. Linares-Barranco and T. Serrano-Gotarredona, "Neuromorphic Spiking Neural Networks and Their Memristor-CMOS Hardware Implementations", Materials, vol. 12, no. 7, article 2745, 2019



Caption: Illustration of massive computing architectures of monolithic CMOS/Memristor neural computing chips assembled on dedicated PCBs.



Caption: Photograph of CMOS chip with memristor test devices fabricated on top.

B. Linares-Barranco, "Memristors fire away", Nature Electronics, vol. 1, no. 2, pp 100-101, 2018

◆ X. Guo, F. Merrikh-Bayat, L. Gao, B.D. Hoskins, F. Alibart, B. Linares-Barranco, L. Theogarajan, C. Teuscher and D.B. Strukov, "Modeling and Experimental Demonstration of a Hopfield Network Analog-to-Digital Converter with Hybrid CMOS/Memristor Circuits", Frontiers in Neuromorphic Engineering, Frontiers in Neuroscience, vol. 9, article 488, 2015

◆ G. Indiveri, B. Linares-Barranco, R. Legenstein, G. Deligeorgis and T. Prodromakis, "Integration of nanoscale memristor synapses in neuromorphic computing architectures", Nanotechnology, vol. 24, no. 38, article 384010, 2013

◆ C. Zamarreño-Ramos, L. A. Camuñas-Mesa, J.A. Perez-Carrasco, T. Masquelier, T. Serrano-Gotarredona and B. Linares-Barranco, "On Spike-Timing-Dependent-Plasticity, Memristive Devices, and building

a Self-Learning Visual Cortex", Frontiers in Neuromorphic Engineering, Frontiers in Neuroscience, vol. 5, article 26, 2011

Key Research Projects & Contracts

Nano-Mind: Neuromorphic Perception and Nano-Memristive Cognition for High-Speed Robotic Actuation
PI: Teresa Serrano Gotarredona
Funding Body: Min. de Ciencia e Innovación
Jun 2020 - May 2024

MeM-Scales: Memory technologies with multi-scale time constants for neuromorphic architectures
PI: Bernabé Linares Barranco
Funding Body: European Union
Jan 2020 - Dec 2022

HERMES: Hybrid Enhanced Regenerative Medicine Systems
PI: Teresa Serrano Gotarredona
Funding Body: European Union
Jan 2019 - Dec 2022

NeuRAM3: NEUral computing aRchitectures in Advanced Monolithic 3D-VLSI nano-technologies
PI: Teresa Serrano Gotarredona
Funding Body: European Union
Jan 2016 - Jun 2019

MemoCiS: Memristors - Devices, Models, Circuits, Systems and Applications
PI: Bernabé Linares Barranco
Funding Body: COST Action IC1401
May 2014 - May 2018

RESEARCH AREA ◆ BIOMEDICAL AND BIOINSPIRED CIRCUITS AND SYSTEMS

Biomedical Circuits and Systems

Contact

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This research line embraces all activities related with the development of alternative bio-instrumentation circuits and systems required to reproduce classical and to propose new measurement techniques at bio-medical labs to improve the quality of acquired biosignals.
Targets design for bio-instrumentation systems are focused also to reduce the human effort and cost of biomedical assays, to obtain the minimum size and weight of biosystems (Lab-on-a-Chips, LoCs), to research new measurement methods based on high performance integrated circuits and system design with low-power consumption, wide bandwidth, reduced power supply levels and wireless communication capability. Electrical modeling of sensors required as signal transducers and interfaces must be incorporated to circuit design flow to obtain full system characterization. This research line also considers the modelling of heterogeneous systems for full system simulations.
Main recent activities are:

- Alternative bio-signals acquisition techniques.
- Development of CMOS circuits and systems blocks.
- To exploit classical sensors and look for new sensor issues for solving biosignals and biomarkers measurement problem.

- Modeling sensor performance and incorporate it into heterogeneous system simulation in a full system design process.

- Development of wearable systems for edema test in heart fail patients.

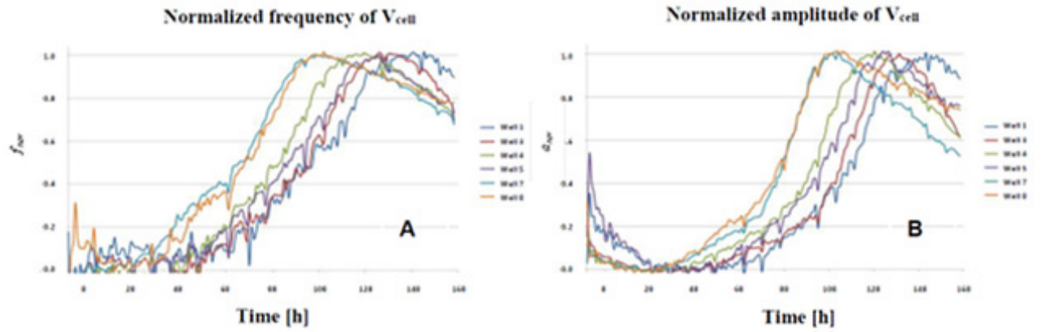
- Electro stimulation of stem cells in differentiation processes.

- Developing multidisciplinary working skills.

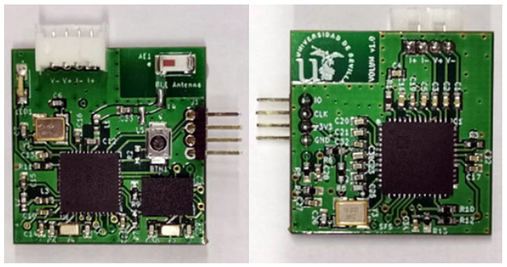
Keywords
Biomedical Circuits and Systems; Bio-Sensors; Laboratory on-a-Chip (LoC); Bioimpedance; Microelectrode; Electro Stimulation (ES); Clinical Applications; Electric Modelling of Biology Systems

Research Highlights

◆ P. Pérez, J.A. Serrano, M.E. Martín, P. Daza, G. Huertas and A. Yúfera, "A computer-aided design tool for biomedical OBT sensor tuning in cell-culture assays", Computer Methods and Programs in Biomedicine, vol. 200, article 105840, 2020



Caption: Normalized frequency (A) and amplitude (B) measured at Vcell in a cell culture. The curves correspond to 2500 cells (W1, W3), 5000 cells (W4, W5) and 10000 cells (W7, W8), seeded at t = 0. Cell proliferation is measured with the oscillation parameters: frequency (fosc) and amplitude (aosc).



Caption: PCB developed for the leg edema test wearable system, to be applied in patients with heart fail disease. The size is set to 2x2 cm2.

◆ J.A. Serrano, P. Pérez, G. Huertas and A. Yúfera, "Alternative general fitting methods for real-time cell-count experimental data processing", IEEE Sensors Journal, vol. 20, no. 24, 2020

◆ P. Pérez, G. Huertas, A. Maldonado-Jacobi, M. Martín, J.A. Serrano, A. Olmo, P. Daza and A. Yúfera, "Sensing Cell-Culture Assays with Low-Cost Circuitry", Scientific Reports, Nature Group, vol. 8, article 8841, 2018

◆ D. Rivas-Marchena, A. Olmo, J.A. Miguel, M. Martinez, G. Huertas and A. Yufera, "Real-time electrical bioimpedance characterization of neointimal tissue for stent applications", Sensors, vol. 17, no. 8, art. 1737, 2017

◆ G. Huertas, A. Maldonado, A. Yufera, A. Rueda and J.L. Huertas, "The Bio-Oscillator: A Circuit for Cell-Culture Assays", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 62, pp. 164-168, 2015

◆ Technology Transfer
Gloria Huertas Sánchez, Andrés Maldonado Jacobi and Alberto Yúfera García. Bioimpedance measurement system for wirelessly monitoring cell cultures in real time, based on an oscillation test using integrated circuits. 2014

◆ Alberto Yúfera García, Alberto Olmo Fernández and Gloria Huertas Sánchez. Bioimpedance measuring system for wirelessly monitoring cell cultures in real time, based on CMOS circuits and electrical modelling. 2014

Key Research Projects & Contracts

SYMAS: Sistema de medida y electroestimulación para aplicaciones de diferenciación y motilidad celular (P18-FR-2308)
PI: Alberto Yúfera García / Gloria Huertas Sánchez
Funding Body: Junta de Andalucía - Proyectos de Excelencia
Jan 2020 - Dec 2022

VOLUM: Valor pronóstico en tiempo real para la monitorización del volumen mediante medidas de bioimpedancias en pacientes con insuficiencia cardíaca aguda (HEART-FAIL VOLUM)
PI: Alberto Yúfera García
Funding Body: Instituto de Salud Carlos III
Jan 2020 - Dec 2021

iSTENT: Real Time Monitoring of Hemodinamic Variables using Smart Stents (iSTENT) based on Capacitive and Bioimpedance Sensors (RTI2018-093512-B-C21)
PI: Alberto Yúfera García
Funding Body: Min. de Ciencia e Innovación
Jan 2019 - Dec 2021

MIXCELL: Integrated MicroSystems for Cell-Culture Assays
PI: Alberto Yúfera García
Funding Body: Min. de Economía y Competitividad
Jan 2014 - Dec 2017

ACATEX: Self-calibration and self-test of analog, mixed-signal and radio frecuency circuits (P09-TIC-5386)
PI: Adoración Rueda Rueda
Funding Body: Junta de Andalucía - Proyectos de Excelencia
Mar 2010 - Feb 2014

Wireless Implantable and Wearable Intelligent Biosensor Devices

Contact

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Research on bioengineering including integrated sensing/read-out circuitry for the detection and recording of neural signals, wearable electronic devices for healthcare monitoring, and efficient wireless interfaces for intelligent medical devices (IMD). The common denominator to these research lines is the need to achieve high precision, low-noise analog read-out and very low power dissipation, in order to enable solutions which can be powered through small-capacity batteries and/or harvesting techniques.
Different activities are being developed in this area:

- Definition of enabling technologies for the integration and miniaturization of biomimetic systems, which can be used for building neurocortical implants suitable for scientific (to allow new advances in neuroscience), clinical (to provide neuroprosthesis for the treatment of neurological diseases), and translational application (to pave the way for brain-machine interfaces) issues.

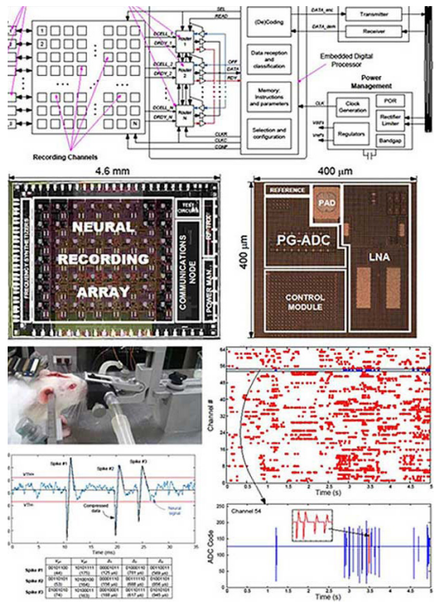
- Development of novel neurological data processing algorithms, including data compression, artifact suppression and seizure prediction processors, suitable for closed-loop therapeutic systems for refractory epilepsy and movement disorder diseases.

- Implementation of wireless sensor nodes (WSN) to quantify the impairments of the neuromuscular function and movement observed in Parkinson disease patients including means of surface electromyography (EMG) or kinematic measurements.

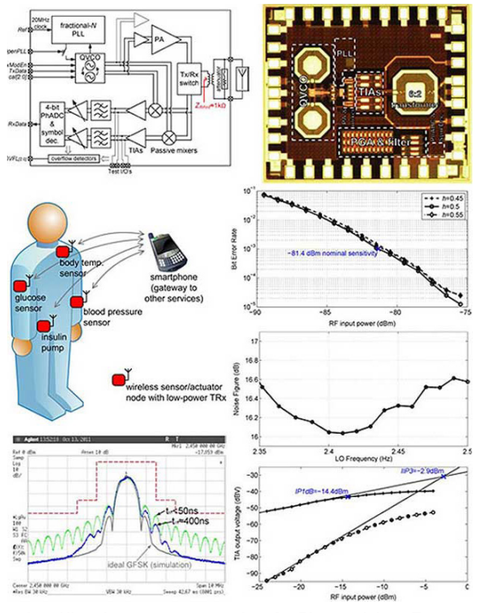
- Fabrication of passive radio-frequency identification (RFID) biomedical sensor tags, including mechanisms for remotely powering, suitable for the acquisition and conditioning of biomedical signals such as body temperature, blood glucose level or ECG information.

- Design of standard-compliant transceivers for wireless body area network (WBAN) applications, including novel architectures and circuit techniques for phase domain modulation.
More details can be found in www2.imse-cnm.csic.es/~mandel/

Keywords
Biomedical Circuits and Systems; Neuro-Engineering; Low-Noise Sensor Readout; Low-Power Wireless Interfaces; Telemetry Systems; Energy Harvesting



Caption: Fully implantable multichannel cortical neural recording system and experimental verification in vivo with animal model.



Caption: Ultra-low power transceiver for Bluetooth Low Energy (BLE). The receiver (Rx) skips any active RF stage and it is implemented as a passive front-end. It achieves a sensitivity of -81.4 dBm and consumes less than 1.1 mW. The transmitter employs direct modulation and an efficient class-E power amplifier (PA) to deliver 1.6 dBm output power to the antenna with a total efficiency of 24.5%.

Research Highlights

◆ R. Fiorelli, M. Delgado-Restituto and Á. Rodríguez-Vázquez, "Charge-Redistribution Based Quadratic Operators for Neural Feature Extraction", IEEE Transactions on Biomedical Circuits and Systems, vol. 14, no. 3, pp. 606-619, 2020

◆ J. L. Valtierra, M. Delgado-Restituto, R. Fiorelli and Á. Rodríguez-Vázquez, "A Sub-µW Reconfigurable Front-End for Invasive Neural Recording that Exploits the Spectral Characteristics of the Wideband Neural Signal", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 5, pp. 1426-1437, 2020

◆ R. Fiorelli, M. Delgado-Restituto and Á. Rodríguez-Vázquez, "Offset-Calibration with Time-Domain Comparators using Inversion-Mode Varactors", IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 1, pp. 47-51, 2020

◆ M. Delgado-Restituto, J. B. Romaine and Á. Rodríguez-Vázquez, "Phase Synchronization Operator for On-Chip Brain Functional Connectivity Computation", IEEE Transactions on Biomedical Circuits and Systems, vol. 13, no. 5, pp. 957-970, 2019

◆ M. Delgado-Restituto, A. Rodríguez-Pérez, A. Darie, C. Soto-Sánchez, E. Fernández-Jover and Á. Rodríguez-Vázquez, "System-Level Design of a 64-Channel Low Power Neural Spike Recording Sensor", IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 2, pp. 420-433, 2017

Key Research Projects & Contracts

MIRABRAS: Millimeter-sized Implant with embedded Responsive Artificial intelligence for Brain disorder Assistance (PID2019-110410RB-I00)
PI: Manuel Delgado Restituto
Funding Body: Min. de Ciencia, Innovación y Universidades
Jan 2020 - Dec 2022

IPANEMA: Integrated Pattern-Adaptive optical NEurostimulator with Multi-site recording Array (TEC2016-80923-P)
PI: Manuel Delgado Restituto
Funding Body: Min. de Economía, Industria y Competitividad
Jan 2017 - Dec 2019

CLEPSYDRA: Towards a Closed-Loop Epileptogenic Prediction SYstem based on sub-Dural Recording Arrays (TEC2012-33634)
PI: Manuel Delgado Restituto
Funding Body: Min. de Economía y Competitividad
Jan 2013 - Dec 2015

POWDERS: Ultra-Low Power Wireless Motes for the Remote Sensing of Biomedical Signals (TEC2009-08447)
PI: Manuel Delgado Restituto
Funding Body: Min. de Ciencia e Innovación
Jan 2010 - Dec 2012

BIO-TAG: Monolithic Implementation of Passive RFID Transponders for Biomedical Applications (TIC-02818)
PI: Manuel Delgado Restituto
Funding Body: Junta de Andalucía
Dec 2007 - Dec 2011

RESEARCH AREA ◆ INTEGRATED CIRCUITS FOR SPACE APPLICATIONS

High-Speed High-Resolution ADCs & DACs for Space Applications

Contact

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This line of research addresses the design of analog and mixed-signal circuits and systems for critical aerospace applications, with emphasis on embedded aerospace applications (satellites, rovers) in CMOS (Complementary Metal-Oxide Semiconductor) technology. These circuits are characterized by being in an environment with high doses of radiation (TID, SE) and need for an autonomous operation without maintenance.
In order to increase the performance and increase the lifespan of these systems, it is necessary to develop and implement Radiation-Hard (Rad-Hard) techniques. In addition and, especially in an application context with little or no possibility of human intervention, these systems should include additional circuitry that capable of automatically measuring and correcting (self-calibration) errors by itself during the entire life of the Instrument (due to the cumulative effect of radiation and aging, as well as change of PVT operating conditions: process, voltage and temperature).

The advantages of research and development of self-calibration techniques are of great importance in critical applications operating under extreme conditions, since the performance of the circuits subjected to stress tend to degrade over time, requiring periodic re-calibrations to preserve the specified operating level.
Another aspect to emphasize is the reliability and reuse of this type of circuits, once developed and qualified, for future missions, which entails a great savings in terms of effort and associated costs.

Keywords
Auto-Calibration; Hardness for Radiation Applications; Embedded Critical Aerospace Applications (Satellites, Rovers, etc.); Sensors; Temperature Sensors; Solar Irradiance Sensors; Mixed Signal ASICs-CMOS for Space

Research Highlights

◆ A.J. Ginés, E.J. Peralías and A. Rueda, "Black-Box Calibration for ADCs With Hard Nonlinear Errors Using a Novel INL-Based Additive Code: A Pipeline ADC Case Study", IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 7, pp. 1718-1729, 2017

◆ J. Núñez, A.J. Ginés, E.J. Peralías and A. Rueda, "Design methodology for low-jitter differential clock recovery circuits in high performance ADCs", Analog Integrated Circuits and Signal Processing, vol. 89, no. 33, pp. 593-609, 2016

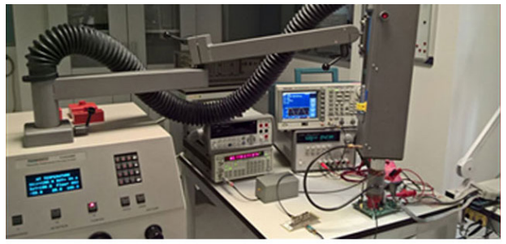
◆ A.J. Ginés, E. Peralías and A. Rueda, "Background Digital Calibration of Comparator Offsets in Pipeline ADCs" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, no. 7, pp. 1345-1349, 2015

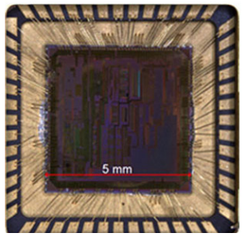
◆ D. Malagon-Perianez, J.M. de la Rosa, R. del Rio and G. Leger, "Single Event Transients trigger instability in Sigma-Delta Modulators", Conference on Design of Circuits and Integrated Systems (DCIS), Madrid, 2014

◆ J. Ramos-Martos, A. Arias-Drake, A. Ragel-Morales, J. Ceballos-Cáceres, J.M. Mora-Gutiérrez, B. Piñero-García, M. Muñoz-Díaz, M.A. Lagos-Florido, S. Espejo-Meana, I. Arruego-Rodríguez, J. Martínez-Oter and M.T. Álvarez, "OWLs: A Mixed-Signal ASIC for Optical Wire-Less Links in Space Instruments", Fourth International Workshop on Analog and Mixed-Signal Integrated Circuits for Space Applications, AMICSA, ESA/ESTEC, Noordwijk, The Netherlands, 2012

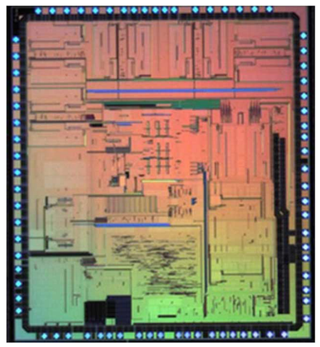
Key Research Projects & Contracts

ASIC-SIS: ASIC for compacts solar irradiation sensor (ESP2016-80320-C2-2-R)
PI: Diego Vázquez García de la Vega
Funding Body: Min. de Economía, Industria y Competitividad
Dec 2016 - Dec 2018





Caption: Test assembly for evaluation of electrical behavior at extreme temperatures. Front microphotograph of the CMOS prototype of the 16bitADC converter.



Caption: Photograph of ASIC CMOS 0.35µm Front-End for solar irradiation sensors on the surface of Mars. The circuit has been designed with the rad-hard library (hardened against radiations) developed at the Microelectronics Institute of Seville (IMSE-CSIC-US).

16BitADC (ESA ITT AO/1-7154 /12/NL/RA)
PI: Juan Ramos (up to 08/2015) / Joaquín Ceballos / Antonio Ginés (from 09/2015)
Funding Body: ESA (European Space Agency)
Sep 2013 - Dec 2015

DANTE: Adapting Mixed-signal and RF ICs Design and Test to Process and Evironment Variability (TEC2011-28302)
PI: Adoración Rueda Rueda
Funding Body: Min. de Ciencia e Innovación
Jan 2012 - Dec 2015

Radiation Tolerant Analogue/Mixed-Signal Technology Survey and Test Vehicle Design (ESTEC Contract No. 400010162110/NL/AF)
PI: José Luis Huertas / Gildas Léger
Funding Body: ESA (European Space Agency) - Through subcontract with ARQUIMEA
Sep 2010 - Sep 2012

System-on-Chip ASICs for Space Instrumentation

Contact

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This line is devoted to the development of integrated circuits and analog/mixed-signal systems for space applications, and in general, for applications in environments suffering radiation and extreme temperatures, with high reliability requirements. The use of conventional CMOS technologies is emphasized, following the concept of radiation hardening by design (RHBD).
Specific activities include the characterization of the effects of high-energy electromagnetic and particles radiation (total ionizing dose –TID, and single-event effects -SEE) on integrated circuit production technologies, on devices and circuits, and the development of robust strategies for the design of circuits and systems. Other topics of interest include the tolerance of circuits to extended temperature ranges, and the resistance of packages and systems to thermal cycles, impacts, and vibration.
Accomplished tasks include:
- Characterization of a 0.35µm CMOS technology concerning radiation effects and extended temperature ranges.

- Development of radiation tolerant digital-cells libraries.

- Development of electrical models for the simulation of MOS transistors with specific radiation-hardened layouts (ELTs).

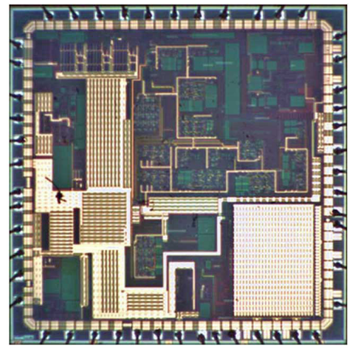
- Design and test of several mixed-signal ASICs for space use.
  · OWLS: intra-satellite optical communications based on diffuse light.
  · MOURA: tri-axial magnetometer and accelerometer.
  · MEDA: wind sensor for MEDA, for Mars'2020.
  · SIS: solar irradiance sensor for Exomars'18.

- Formal qualification processes for the space-use of mixed-signal ASICs.

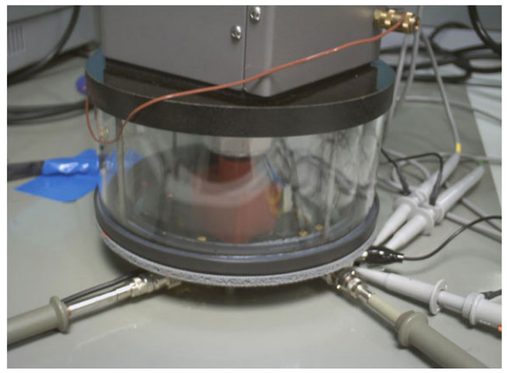
Keywords
Radiation Hardening; Extended Temperature Ranges; Reliability; Total Ionizing Dose; Single-Event Effects; Redundancy; Latch-up Prevention

Research Highlights

◆ S. Sordo-Ibáñez, B. Piñero-García, M. Muñoz-Díaz, A. Ragel-Morales, J. Ceballos-Cáceres, L. Carranza-González, S. Espejo-Meana, A. Arias-Drake, J. Ramos-Martos, J.M. Mora-Gutiérrez and M.A. Lagos-Florido, "CMOS Rad-Hard Front-End Electronics for Precise Sensors Measurements", IEEE Transactions on Nuclear Science, vol. 63, pp. 2379-2389, 2016



Caption: ASIC OWLS



Caption: ASIC for MEDA wind sensor

◆ S. Sordo-Ibáñez, B. Piñero-García, M. Muñoz-Díaz, A. Ragel-Morales, J. Ceballos-Cáceres, L. Carranza-González, S. Espejo-Meana, A. Arias-Drake, J. Ramos-Martos, J.M. Mora-Gutiérrez and M.A. Lagos-Florido, "A Front-End ASIC for a 3-D Magnetometer for Space Applications by Using Anisotropic Magnetoresistors", IEEE Transactions on Magnetics, vol. 51, pp. 1-4, 2015

◆ S. Sordo-Ibáñez, S. Espejo-Meana, B. Piñero-García, A. Ragel-Morales, J. Ceballos-Cáceres, M. Muñoz-Díaz, L. Carranza-González, A. Arias-Drake, J.M. Mora-Gutiérrez, M.A. Lagos-Florido and J. Ramos-Martos, "Four-channel self-compensating single-slope ADC for space environments", Electronics Letters, vol. 50, pp. 579-581, 2014

◆ J. Ramos-Martos, A. Arias-Drake, J.M. Mora-Gutiérrez, M. Muñoz-Díaz, A. Ragel-Morales, B. Piñero-García, J. Ceballos-Cáceres, L. Carranza-González, S. Sor-

do-Ibáñez, M.A. Lagos- Florido and S. Espejo-Meana, "SEE Characterization of the AMS 0.35 µm CMOS Technology", in Proc. of the 14th European Conf. on Radiation and its Effects on Components and Systems, pp. 1-4, 2013

◆ J. Ramos-Martos, A. Arias-Drake, A. Ragel-Morales, J. Ceballos-Caceres, J.M. Mora-Gutierrez, B. Pinero-Garcia, M. Munoz-Diaz, M.A. Lagos-Florido and S. Espejo-Meana, "Radiation Characterization of the austriamicrosystems 0.35 µm CMOS Technology", in Proc. of the 12th European Conf. on Radiation and its Effects on Components and Systems, 2011

Key Research Projects & Contracts

Microelectrónica para instrumentación espacial: ASIC del sensor de viento de MEDA (ESP2016-79612-C3-3-R)
PI: Servando Espejo Meana
Funding Body: Min. Economía y Competitividad
Jan 2017 - Dec 2018

Microelectrónica de espacio para instrumentación ambiental en Marte (ESP2014-54256-C4-4-R)
PI: Servando Espejo Meana
Funding Body: Min. Economía y Competitividad
Jan 2015 - Dec 2015

Diseño y testado de ASICs para el espacio para la misión a Marte 'MEIGA-METNET Precursor' (AYA2011-29967-C05-05)
PI: Servando Espejo Meana
Funding Body: Min. de Ciencia e Innovación
Jan 2012 - Dec 2012

Diseño y testado de ASICs para el espacio para la misión a Marte 'MEIGA-METNET Precursor' (AYA2009-14212-C05-04)
PI: Servando Espejo Meana
Funding Body: Min. de Ciencia e Innovación
Jan 2010 - Dec 2011

Diseño y testado de ASICs para el espacio para la misión a Marte 'MEIGA-METNET Precursor' (AYA2008-06420-C04-02/ESP)
PI: Servando Espejo Meana
Funding Body: Min. de Ciencia e Innovación
Jan 2009 - Dec 2009

RESEARCH AREA ◆ HARDWARE SECURITY

Cybersecurity

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This research line focuses on microelectronic solutions for security applications. The objectives are to verify the identity of hardware devices and users as well as to store and communicate sensitive information, resorting to the use of techniques from cryptography, biometrics, and their combination (crypto-biometrics). Security against hardware attacks is especially analyzed, particularly fault injection and side-channel attacks such as differential power analysis (DPA) and differential electromagnetic attacks (DEMA). Microelectronic solutions are aimed at constructions and algorithms providing security together with efficient features of size, power consumption and operation speed.
The activities within this research line are devoted to:
- Exploration of cryptographic algorithms from a secure hardware implementation point of view. Development of architectures for such algorithms with optimized features in terms of VLSI design and resistance against attacks.

- Analysis of side-channel and fault-injection attack sources. Development of robust hardware solutions as well as setups and benchmarks to measure the security of microelectronic realizations against attacks. Vulnerability metrics.

- Design of modules based on PUFs (within programmable devices and/or integrated circuits) to implement security primitives particularly related to key generation, identifiers, and random numbers.

- Hardware implementation of algorithms to process and recognize biometric features such as fingerprints, faces, gait, voice, etc. Design of microelectronic solutions for biometric, multi-biometric, and crypto-biometric systems.

- Application of the above solutions to wearable devices, tokens, tags, consumer electronic devices, control systems, etc.

Keywords
Hardware for Cryptography; Biometrics and Crypto-Biometrics; Physical Unclonable Functions (PUFs); Secure FPGAs and Integrated Circuits; Hardware Attacks; Authentication and Secure Communications

Research Highlights

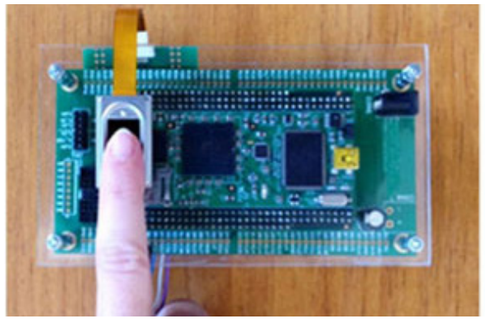
◆ J.M. Mora-Gutiérrez, C.J. Jiménez-Fernández and M. Valencia-Barrero, "Trivium Hardware Implementations for Power Reduction", International Journal of Circuit Theory and Applications, Special Issue: Secure lightweight crypto-hardware, vol. 45, no. 2, pp. 188-198, 2017

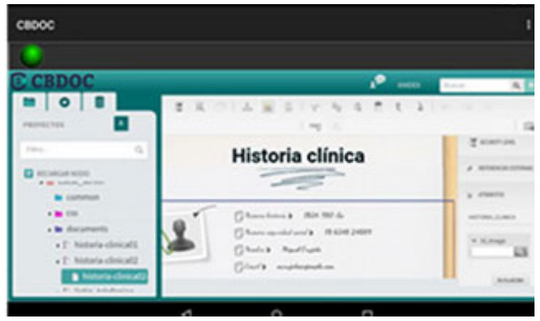
◆ A. Cabrera-Aldaya, A.J. Cabrera and S. Sánchez-Solano, "SPA Vulnerabilities of the Binary Extended Euclidean Algorithm", Journal of Cryptographic Engineering, vol 7, no. 4, pp. 273-285, 2017

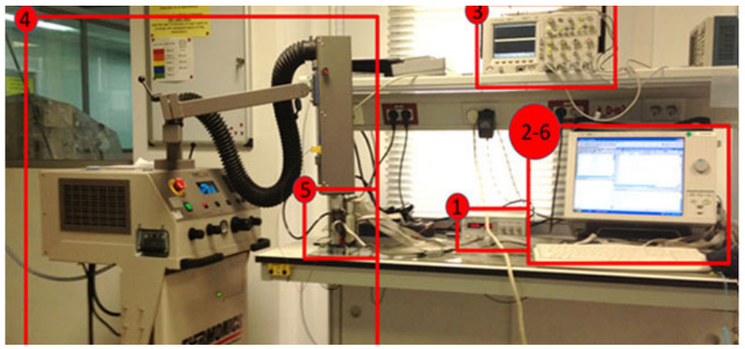
◆ I. Baturone, M.A. Prada-Delgado and S. Eiroa, "Improved generation of identifiers, secret keys, and random numbers from SRAMs", IEEE Transactions on Information Forensics and Security, vol. 10, no. 12, pp. 2653-2668, 2015

◆ E. Tena-Sánchez, J. Castro and A.J. Acosta, "A Methodology for Optimized Design of Secure Differential Logic Gates for DPA Resistant Circuits", IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 4, no. 2, pp 203-215, 2014

◆ R. Arjona and I. Baturone, "A Hardware Solution for Real-Time Intelligent Fingerprint Acquisition", Journal of Real-Time Image Processing, vol. 9, no. 1, pp. 95-109, 2014







Caption: Prototype of e-padlock which allows dual-factor authentication (what you have and who you are) in the access to a content management system.

Caption: Experimental setup to measure hardware security: 1.- Power supply, 2.- Logic analyzer, 3.-Oscilloscope, 4.- Temperature control system, 5.- Device under test, 6.- Software to automate measurements.

Key Research Projects & Contracts

INTERVALO: Integración y validación en laboratorio de contramedidas frente a ataques laterales en criptocircuitos microelectrónicos (TEC2016-80549-R)
PI: Antonio J. Acosta Jiménez / Carlos J. Jiménez Fernández
Funding Body: Min. de Economía y Competitividad
Dec 2016 - Dec 2019

SENIAC: Security in interconnected devices by injection of authentication and ciphering algorithms (RTC-2014-2932-8)
PI: Iluminada Baturone Castillo
Funding Body: Min. de Economía y Competitividad
Oct 2014 - Mar 2017

CESAR: Secure microelectronic circuits against side-channel attacks (TEC2013-45523-R)
PI: Antonio J. Acosta Jiménez / Carlos J. Jiménez Fernández
Funding Body: Min. de Economía y Competitividad
Jan 2014 - Dec 2016

CB-DOC: Content management system with secure authentication by cripto-biometric techniques based on hardware (IPT-2012-0695-390000)
PI: Iluminada Baturone Castillo
Funding Body: Min. de Economía y Competitividad · Proyecto INNPACTO
Jul 2012 - Mar 2015

CRIPTO-BIO: Microelectronic design for crypto-biometric authentication (P08-TIC-03674)
PI: Iluminada Baturone Castillo
Funding Body: Junta de Andalucía - Proyectos de Excelencia
Jan 2009 - Dec 2013

Security and Reliability in CMOS and Emerging Technologies

Contact

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The development of IoT in the near future faces numerous technological challenges that need to be addressed, such as power/energy efficiency, reliability, security, and cost. Advanced CMOS technologies are potential candidates for solutions in the short term to those challenges, whereas beyond-CMOS devices are the answer for solutions in the long term. All these technologies are plagued with both time-zero and time-dependent variability effects. From a reliability point of view, design strategies and methodologies are required to deal with the mitigation or tolerance to variability effects. But from an exploitation perspective, variability can be regarded as an advantage rather than as a problem, e.g. in the hardware security field.
This research line focusses in the development of new and robust Physical Unclonable Functions and lightweight cryptographic solutions combining the experience of researchers in reliability characterization and reliability-aware design in CMOS technology and low-power circuit design in beyond-CMOS technologies. More specifically, the work includes activities in the following design areas:
- Design of Physical Unclonable Functions: Exploitation of time-zero and time-dependent variability effects in microelectronic devices for security applications.
- Reliability
  · Characterization and modeling of time-zero and time-dependent variability effects in micro/nano-electronic devices.
  · Robustness of lightweight cryptographic solutions.
- Low-power circuit design in beyond-CMOS technologies.

Keywords
Hardware Security; PUF; Lightweight Cryptography; Reliability; Variability Effects; Beyond-CMOS Devices

Research Highlights

◆ P. Saraza-Canflanca, H. Carrasco-Lopez, A. Santana-Andreo, P. Brox, R. Castro-Lopez, E. Roca and F.V. Fernandez, "Improving the reliability of SRAM-based PUFs under varying operation conditions and aging degradation", Microelectronics Reliability, vol. 118, article 114049, 2021.

◆ P. Saraza-Canflanca, J. Martin-Martinez, R. Castro-Lopez, E. Roca, R. Rodriguez, F.V. Fernández and M. Nafria, "Statistical characterization of time-dependent variability defects using the máximum current fluctuation", IEEE Transactions on Electron Devices, vol. 68, no. 8, pp 4039-4044, 2021

◆ J. Díaz-Fortuny, P. Saraza-Canflanca, R. Castro-Lopez, E. Roca, J. Martin-Martinez, R. Rodriguez, F.V. Fernández and M. Nafria, "Flexible Setup for the Measurement of CMOS Time-Dependent Variability with Array-Based Integrated Circuits", IEEE Transactions on Instrumentation and Measurement, vol. 69, no. 2, pp 853-864, 2020

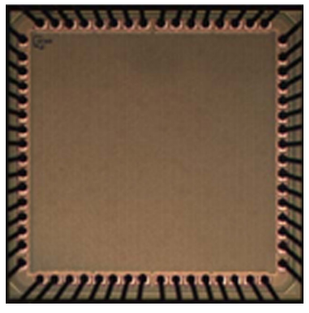
◆ I.M. Delgado-Lozano, E.Tena-Sánchez, J. Núñez and A. Acosta, "Design and analysis of secure emerging crypto-hardware using HyperFET devices", IEEE Transactions on Emerging Topics in Computing, vol. 9, no. 2, pp 787-796, 2020

◆ J. Diaz-Fortuny, J. Martin-Martinez, R. Rodriguez, R. Castro-Lopez, E. Roca, X. Aragonés, E. Barajas, D. Mateo, F.V. Fernandez and M. Nafria, "A Versatile CMOS Transistor Array IC for the Statistical Characterization of Time-Zero Variability, RTN, BTI and HCI", IEEE Journal of Solid-State Circuits, vol. 54, no. 2, pp 476-488, 2019

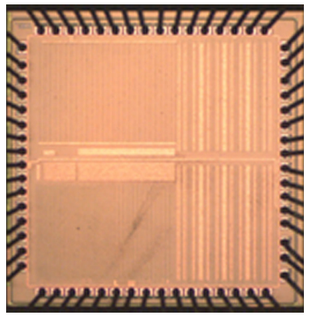
Key Research Projects & Contracts

VIGILANT: The Variability Challenge in Nano-CMOS - SUB-PROJECT MITIGATION (PID2019-103869RB-C31)
PI: Francisco V. Fernández Fernández / Rafael Castro López
Funding Body: Min. de Ciencia, Innovación y Universidades
Jun 2020 - May 2023

TOGETHER: Towards Trusted Low-Power Things: Devices, Circuits and Architectures (TEC2016-75151-C3-3-R)
PI: Francisco V. Fernández Fernández / Rafael Castro López
Funding Body: Min. de Economía, Industria y Competitividad
Jan 2017 - Jun 2021



Caption: ENDURANCE: Chip design for the statistical characterization of time-dependent variability at device level. It includes four large arrays of CMOS transistors.



Caption: KIPT: Chip design for the statistical characterization of time-dependent variability at circuit level. It includes four large arrays of cells or circuit blocks: one array of SRAM and Sense Amplifier, one array of Analog Circuits and two of Ring Oscillators.

FOUNDED PROJECTS

NATIONAL GOVERNMENT
- ARES
- HARDWALLET
- MAS+CARA
- NANO-MIND
- CORDION
- MIRABRAS
- VIGILANT
- VOLUM
- HEART-FAIL VOLUM
- ENVISAGE
- MEDACAL-SPHERE
- ISTENT
- ASICS-AVATART
- STATSET
- HARDBLOCK
- HW-IDENTIOTY
- PULPOSS
- TOGETHER

REGIONAL PROJECTS
- VERSO
- COGNITIO
- SYMAS
- SPADARCH
- INFRAESTRUCTURA 5169
- CRYPTOHARDWEAR
- TRANSFERENCIA CONOCIMIENTO
- CEI
- OFICINA PROYECTO

EUROPEAN UNION
- SPIRS
- SPINAGE
- APPROVIS3D
- NEURONN
- MEM-SCALES
- HERMES
- ACHIEVE

CSIC PROJECTS
- I-COOP+ 2019
- I-LINK 2019

NATIONAL GOVERNMENT

ARES

Design, implementation and validation of attack-resistant hardware roots of trust for secure embedded systems.

PI: **Carlos J. Jiménez Fernández** cjesus@imse-cnm.csic.es
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Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Ref: **PID2020-116664RBI00**
Start date: 01/09/2021 End date: **31/08/2025**
Funding: **146.410,00 €**

The inclusion of secure elements in embedded devices is improving in current available commercial solutions. Some manufacturers offer solutions to protect their products against cybersecurity threats. However, the restricted hardware resources of certain devices (e.g. in the Internet-of-Things context) make unfeasible the adoption of some of these complex protection schemes such as Trusted Platform Modules. The design of a Root-of-Trust (RoT) using low-cost hardware modules is presented in this project as alternative. The RoT is conceived as cornerstone, thus deriving trust for the rest of components that compose the embedded system. The RoT will be designed to be a modular, configurable and adaptable structure, thus leveraging the resources to offer dedicated solutions for each particular application case.

The tendency of open source initiatives for embedded systems has been consolidated with the advent and rapid growth of the RISC-V Instruction Set Architecture (ISA) together with its comprehensive hardware and software ecosystems. However, the open nature of RISC-V ISA is a double edged-sword for security purposes. The flexibility of the instruction set allows the possibility of developing various cryptography-specific

extensions or variants of the ISA with the aim of increasing the level of security.

But at the same time, the full-access to many 'open-hardware' implementations of the RISC-V ISA could expose them to more vulnerabilities compared to the proprietary world where this information is hidden and protected by strong Intellectual Property rights. Therefore, the development of solutions to foster the security of embedded systems based on this ISA is an open challenge for research community. This project will increase the security of embedded RISC-V systems by incorporating a RoT anchored in the device's own hardware. This strategy will be also adapted to be used by cores with proprietary ISA, thus allowing to establish a performance comparison between both choices (open and non-open) for embedded systems.

The general objective of the ARES project is to provide hardware solutions to improve the security of embedded systems, designing a hardware RoT that includes cryptographic primitives for secure storage, processing and transmission of data. The building components of the RoT will be Physical Unclonable Functions (PUFs) to generate the identity of the electronic device and generate cryptographic keys as well as entropy sources, and cryptographic primitives for data encryption and decryption. All these elements will include measures to verify its correct behavior and countermeasures to prevent physical attacks. Implementations will be carried out in both FPGA and ASIC technology, using ARM and RISC-V processors, suitable to be used in Internet-of-Things (IoT) technology. For the sake of validation, the project will develop a demonstrator to leverage project advances in a sector as eHealth where security is crucial.

HARDWALLET

Trusted, Post-Quantum Secure Hardware for Decentralized Identity Wallets Using Distinctive Traits of People and Devices.

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M. Rosario Arjona López arjona@imse-cnm.csic.es

Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Ref: **PID2020-119397RB-I00**
Start date: 01/09/2021 End date: **30/08/2024**
Funding: **83.853,00 €**

Electronic identification allows entities to prove electronically that they are who they say they are in order to access services and carry out electronic transactions. Identity verification uses identifiers, which are uniquely associated with entities, and verification mechanisms that prove the association between the entity and its identifiers. In decentralized identity systems, entities have complete control of their identifiers. Entities are the owners and issuers of their identity (there are no centralized registries, no identity providers, no certification authorities to assign identities as centralized and federated systems do).

Distributed ledger technology, including blockchains, or some other form of decentralized network, enables identity verification using cryptography. Currently, the most established method for verification employs digital signatures. The entity is the only one that has a private key associated with a public key. The most secure solution locally generates its own private and public key pair so that the private key is truly private. Therefore, the genuine entity is the only one capable of generating signatures with its private key and any other entity can verify the signatures with the public key. The decentralized network stores public identifiers and public keys, The current W3C draft on Decentralized IDentifiers (DIDs) includes verification mechanisms, such as public keys and pseudonymous biometrics, that the owner can use to prove their association with the DID. However, most applications verify an individual by applying biometrics locally. No external verifier can prove that the individual actually participates in the process. The reason is that practical and efficient implementations of pseudonym biometrics that offer irreversibility, unlinkability and revocability are still a challenge in decentralized networks.

The HardWallet Project will address the challenge of verifying pseudonymous biometrics externally, meeting demand from Europe and the United States for a decentralized and better privacy-preserving approach. As the IoT and artificial intelligence are producing more and more autonomous electronic devices that conduct electronic transactions as an individual, the HardWallet project will extend verification externally to physical devices with unique electronic characteristics using PUFs (Physical Unclonable Functions). cloneable).

Nowadays, the hardware solutions used in digital wallets to manage private keys and guarantee the integrity of the platform, the confidentiality of the data stored in a non-volatile memory and the authenticity of the executed code (in charge of locally verifying the biometric data sensitive) use classical cryptography. The HardWallet Project will develop secure and reliable hardware to also generate pseudonyms from biometrics and device metrics. In addition, to guarantee long-term security, the cryptography used in the wallet will be post-quantum.

MAS+CARA

Proof of concept of a decentralized facial recognition scheme, offering privacy and post-quantum security.

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Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Ref: **PDC2021-121589-I00**
Start date: 01/12/2021 End date: **30/11/2023**
Funding: **104.650,00 €**

Nowadays, interactions are moving from face to face in the physical world to the Internet. Electronic instead of physical interactions are growing meteorically. Consequently, electronic identification is a booming market since it allows people to prove electronically that they are who they say they are in order to gain access to services or carry out electronic transactions.

Typically, a person proves: (a) to know secret data whenever the verifier asks what you know, (b) to have a unique possession (what you have), and (c) to be a physical entity (who you are). In the last case, people usually provide biometric data, such as data from their faces. Biometric data, which are stored as template at the registration phase or enrollment, are private and sensitive data, as contemplated in the data protection regulation of many countries. Hence, protection schemes should be employed to transform them into public non-sensitive data named pseudonyms. The problem is that, concerning a brute-force attack, the security of current biometric recognition systems usually ranges from 17 to 24 bits. This is very much lower than the security of a cryptographic system (80 bits at least). Moreover, the biometric schemes with template protection offer even lower security. Recently, new cryptographic techniques, like homomorphic encryption, are being explored to increase the security of protected biometric recognition systems. However, the security of many of these techniques is based on problems (like the Discrete Logarithm and the Integer Factorization problems) that are hard for current computers but not for quantum computers, which will be available in the future. Thanks to the results obtained in our previous project TEC2017-83557-R, the project Mas+Cara will develop protected schemes using post-quantum cryptog raphy to offer a high and long-term security. Nowadays, most of electronic identification systems employ a device-centric authentication topology, in which the PIN (what you know) or the biometric (who you are) data capture and processing (feature extraction and matching), as well as the storing of the biometric templates, are all handled locally, on the users device (what you have). The most widely extended device is the smartphone. The device authenticates its user. The person is who its device says he/she is without any external verification. No external verifier can attest that a credential holder (a person) is truly presenting a digital credential.

Recently, new protected schemes using a decentralized model are being explored to ensure that the digital credentials can be verified externally by using public keys and pseudonymous biometrics that could offer people privacy. However, while the cryptographic verification of digital signatures with public keys is quite well established, the efficient and practical implementations of pseudonymous biometrics offering irreversibility, unlinkability, and revocability are still a challenge.

Exploiting the knowledge acquired in our previous project TEC2017-83557-R, the project Mas+Cara will develop protected schemes using post-quantum cryptography and a decentralized and private model. The proof of concept to be developed in Mas+Cara will be implemented by means of smartphone App and will be validated in a relevant environment so that a prototype will be ready to be demonstrated in an operational environment and the way will be paved to obtain a final product to commercialize.

NANO-MIND

Neuromorphic Perception and NANO-Memristive CognItioN for High-SpeeD Robotic Actuation

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Projects Details
Type: **Research project**
Funding Body: **Ministerio de Ciencia, Innovación y Universidades**
Reference: **PID 2019-105556GB**
Start date: 01/06/2020
End date: **31/05/2024**
Funding: **208.770,00 €**

In the last years, due to the availability of large amounts of annotated data and the increase of the computation capability of highperformance computing platforms, we have witnessed a resurgence of artificial intelligence (AI) and neuro-inspired computation. AI systems outperforming human beings in image classification tasks have been demonstrated. However, those systems still lag well behind human beings if we compare them in terms of speed and energy efficiency. The intensive computation requirements of AI recognition systems cause that the developed AI systems for our portable devices perform computations on the cloud. It has been foreseen that by the year 2025, one-fifth of the world's electricity will be consumed by the internet.
The development of efficient information coding schemes and low power AI hardware platforms is a must if we want to witness the spreadof AI systems while keeping an affordable energy budget. Current state-of-the-art AI systems are based on an information coding and processing paradigm which is quite different from the

way biological brains code and process the information. If we consider vision as an example, state-of-the-art AI computational vision systems code and process the information as sequences of static frames. However, biological neurons produce and communicate sequences of spikes. In this context, the so-called third generation of neural networks or spiking neural networks has emerged to emulate the efficiency in information coding and computation of human brains.
However, spiking neural networks computational systems lack the maturity of frame-based conventional computing systems in terms of theoretical development, learning and controlling algorithms and availability of event-based sensors, event-based hardware computing platforms, and event-based robotic actuators.

The NANO-MIND project aims to advance in the theoretical and hardware development of neuromorphic spiking neural systems from the sensors level, to the processing level up to the control and actuation level.

CORDION

Digitizers based on Cognitive Radio for IoT nodes.

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Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Reference: **PID2019-103876RB-I00**
Start date: 01/06/2020 End date: **31/07/2024**
Funding: **55.902,00 €**

IoT (Internet of Things) implies the interconnec- tion of billions of cyberphysical entities, capable of communicating with each other, without the need lor human intervention, also relerred to machine- to-machine communication. However, the practi- cal implementation of IoT requires also the deve- lopment of electronic devices that are secure and efficient in terms of cost and energy consumption. They also need to be equipped with a certain level of intelligence giving rise lo the so-called smart de- vices/objects and autonomy, so that they can make decisions in real time, and locally, i.e. withoul being connected to remate servers.

The so-called Cognitive Radio (CR) technology allows communication systems to make a more efficient use of the electromagnetic spectrum, by dynamically modifying its transmission and re- ception parameters according to the information sansed from the environment a technique also re- ferred to as spectrum sensing. One of the direct consequences of the physical implementations of CR-based terminals is that the digitizers, i.e. the circuits responsible for transforming the signal from the analog to the digital domain, should be placed as clase as possible to the antenna, so that most of the hardware is digital and hence, it is easier to program vía software.

Another key technology enabler for the develop-ment of CR-based IoT nodes is the need to embed a certain degree of Artificial Intelligence (AI), so that they can set their specifications in an optimum and autonomous way, according to the environment conditions (communication coverage, spectrum oc- cupancy, intereferences), battery status and energy consumption.

In this scenario, this project aims to address some of the design challenges for the increased in-coming digital-driven world directly linked to the Economía, Sociedad y Cultura Digitales, which is one of the priority challenges of the Plan Estatal 2017- 2020. To this end, AI-managed digitizers for CR-based IoT nodes will be developed in this project.

INFRASTRUCTURE PROJECT

Update of the analysis and signal generation equipments features for the challenges of the next technological leap in micro and nano-electronics.

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Projects Details:
Type: **Research project**
Funding Body: **MICIN**
Reference: **EQC2021-007363-P**
Start date: 01/06/2021 End date: **31/12/2023**
Funding: **904.000€**

The aim of this action is to update the equipment of the Technical Support service for the Design and Test of Integrated Circuits of the Institute of Microlectronics of Seville to face the challenges of the next technological leap in Micro and Nanoelectronics. Among the new challenges are the better use of the electromagnetic spectrum for the widespread expansión of 5G and the Internet of Thing (IoT), its combination with Artificial Intelligence (AioT), improvements in IoT security or more efficient and faster digitizers.

New equipment will allow the development of areas with great future projection, such as cybersecurity or the coexistence of quantum computing and conventional electronics, which will require ultra-high-speed devices to bond both paradigms. The new interest in space exploration will also promote Micro and Nanoelectronics in space, an area in which there is already experience in the development and testing of circuits for missions such as Curiosity and Perseverance, and which will also be enhanced by this action and encouraging participation in new missions.

From the socio-economic point of view, the new equipment will promote the creation of new patents and new technology-based companies for their exploitation, with the direct creation of very high-quality employment in a geographical area with high unemployment rates, justifying fully the investment made.

MIRABRAS

Millimeter-sized Implant with embedded Responsive Artificial intelligence for Brain disorder Assistance

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Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia e Innovación**
Reference: **PID2019-110410RB-I00**
Start date: 01/06/2020
End date: **31/05/2023**
Funding: **137.819,00 €**

This Project aims to provide enabling microelectronic technologies for the integration and miniaturization of a smart implantable neural stimulation system, which serves as experimental vehicle for the development of new procedures in neurophysiology and, ultimately, for the implementation of new neural prosthesis, more focus and safe than those currently available, for the understanding and treatment of different pathologies of the nervous system, with emphasis in brain disorders, such as including Alzheimers disease, epilepsy or Parkinsons disease.

In particular, this Project will explore emerging approaches for treating neural disorders in which regenerative medicine techniques (interneuron transplants expressing regenerative promoters) are combined with optogenetics stimulation. In this application, small implantable neural interface devices in millimeter-scale are needed to deliver light stimuli and interact with the transplant for attenuating disease pathologies. Compared to electrical stimulation, the optogenetic approach allows selectively exciting individual cells with very high spatial and temporal accuracy, leaving the rest of the cells intact and, thus, reducing side effects.

In another aspect, the Project will advance towards the practical implementation of a reliable and efficient closed-loop mechanism which, based on the electrical activity recorded from the genetically encoded cells, is able to provide an efficient and non-harmful actuation by optical means. This real-time feedback procedure will support the adaptability of the system to the plasticity of the neural tissue and, thereby, it will open up doors for the implementation of robust, long lifetime neural prosthesis whose operation self-adjusts to the patient's progress. In order to improve the selectivity and detection accuracy of the closed-loop system, Artificial Intelligence (AI) paradigms will be explored seeking an optimum equilibrium between efficiency and hardware cost.

Also, to favor miniaturization, the Project will investigate the integration of fully wireless solutions in the implant both for data and power transfer. Through analysis, simulation, and measurements on prototypes, different coil structures will be explored for powering mm-sized neural interfaces, paying attention to keep the Specific Absorption Rate (SAR) of electromagnetic (EM) field in the tissue under safe limits.

VIGILANT

The Variability Challenge in Nano-CMOS: From Device Modeling to IC Design for Mitigation and Exploitation

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Type: **Research project**
Funding Body: **Ministerio de Ciencia, Innovación y Universidades**
Reference: **PID2019-103869RB-C31**
Start date: 01/06/2020
End date: **31/05/2023**
Funding: **117.491,00 €**

Electronic devices flood many aspects of our lives. The wondrous evolution of nano-CMOS technologies with the emergence of new materials and devices is behind it. The demand for integrated circuits (ICs) is not without challenges though: our modern digital economy and society requires them to be more functional, more reliable, safer and more secure, and fields like IoT, Cybersecurity and Highperformance computing are now priorities in many research agendas.

However, one critical obstacle in this evolution is variability, culprit for the device parametric fluctuations deriving in a reliability loss of the IC. Rising right after fabrication (TZV, Time-Zero Variability) or during the IC lifetime (TDV, Time-Dependent Variability), it ends up critically compromising its functionality or even cutting short its lifetime. If variability is undealt with, ICs will no longer be able to fulfil the capabilities of safety, security, and reliability.

VIGILANT faces up this challenge from two perspectives. It will first develop solutions and new de-

sign paradigms to lessen or tolerate variability; the goal is clear: mitigate its negative impact. Second, realizing variability has also a beneficial side, TZV and TDV will be exploited for hardware-based security. While this duality mitigation/exploitation is one key goal, there is another cross-cutting goal: the evaluation of several technologies and their potential for the duality, from the established bulk CMOS, through the versatile FDSOI, to beyond-CMOS alternatives like memristors. To undertake the goals, VIGILANT needs the complementary expertise of teams (IMSE, UAB and UPC) with a successful track record in the collaborative investigation of variability.

VOLUM

Prognostic value of real-time body volumes monitoring by continuous bioimpedance measurement in patients with acute heart failure (HEART-FAIL VOLUM)

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Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia, Innovación y Universidades**
Reference: **DTS19/00134**
Start date: 01/01/2020
End date: **31/12/2021**
Funding: **46.200,00 €**

Heart failure (HF) is the currently leading cause of hospitalization in people over 65 years in Europe. The standard evaluation of this disease does not reliably predict HF outcome. Volume overload due to neuro-hormonal activation is the primary factor leading to HF hospitalisation, and volume measurements by bioimpedance (BI) have preliminary shown to be useful for diagnosis and prognosis. However, the measures are performed punctually, or in a short period, but the dynamics of fluid overload in patients with acute HF during hospitalisation and after discharge have not been previously described. The aim of this study is evaluate the prognostic value of monitoring changes in body volumes by continuous BI measurement with a novel wearable device to predict early clinical outcome in patients with acute HF.

HEART-FAIL VOLUM

Valor pronóstico en tiempo real para la monitorización del volumen mediante medidas de bioimpedancias en pacientes con insuficiencia cardíaca aguda

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Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia, Innovación y Universidades**
Reference: **DTS19/00134**
Start date: 01/01/2020
End date: **21/12/2021**
Funding: **46.200,00 €**

La insuficiencia cardíaca (IC) es la principal causa de hospitalización en personas mayores de 65 años en Europa. La evaluación clínica estándar no permite predecir de forma fiable la evolución de esta enfermedad. La sobrecarga de volumen debido a la activación neuro-hormonal es el principal factor implicado en las hospitalizaciones por IC, y las mediciones de los volúmenes corporales por bioimpedancia (BI) han demostrado de manera preliminar que son útiles en el diagnóstico y pronóstico. Sin embargo, las medidas se realizan puntualmente, o en un período corto, pero la dinámica de la sobrecarga de líquidos en pacientes con IC aguda durante la hospitalización y tras el alta no se han descrito previamente. El objetivo de este estudio es evaluar el valor pronóstico de la monitorización de los volúmenes corporales en tiempo real mediante la medición continua de BI con un nuevo dispositivo portátil para predecir precozmente la evolución clínica en pacientes con IC aguda.

ENVISAGE

Enabling Vision Technologies for Integrated Intelligent Transportation

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Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia, Innovación y Universidades**
Reference: **RTI2018-097088-B-C31**
Start date: 01/01/2019
End date: **30/06/2022**
Funding: **144.958,00 €**

The objective of this project is the development of embedded vision systems for intelligent transport. The aim is to capture the specificities of this field of application and incorporate them into a holistic design flow. In this way, we will develop embedded vision systems adapted for autonomous platforms and vehicles and to be incorporated to the traffic control and monitoring infrastructure. The main challenge will be the implementation of an important amount of computing power under a restricted power budget. The conventional approach, in which the different components are developed separately from specifications derived from a high-level description, can be inefficient, leading to sub-optimal performance. Our approach consists of multi-parametric and multi-level optimization.

We will develop a system description tool that will allow us to navigate the hierarchy of the vision system and propagate specifications and restrictions from the device- to the application-level and vice versa.

MEDACAL-SPHERE

MEDA Wind Sensor Calibration and Spherical Wind Sensor ASIC

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Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia, Innovación y Universidades**
Reference: **RTI2018-098728-B-C32**
Start date: 01/01/2019
End date: **31/12/2021**
Funding: **176.055,00 €**

Sub-project MEDACAL-SPHERE has two specific objectives within the coordinated project. Both objectives are connected among them. The first one is to contribute and support the measurements, calibration, and the interpretation of the data obtained from the MEDA wind sensor, which uses a mixed-signal ASIC designed using radiation hardening by design techniques and which performs the conditioning, acquisition and conversion of the sensor signals. This ASIC was developed by the research team in the framework of previous research projects (the MEDA wind-sensor ASIC). The second objective is the design, fabrication and validation of a new mixed-signal ASIC for a new generation of the wind sensor, the so called spherical wind sensor, developed like the previous one by the Polytechnic University of Catalonia. This new version of wind sensor, more accurate than the previous one, will be used as a reference element for the fine calibration of the MEDA wind sensor, which will be sent to Mars, therefore connecting with the first objective. As a result, this new ASIC,which constitutes the second objective, will have the double function of completing the development of the new generation of spherical wind sensors, and serve as a reference for the detailed calibration of the sensors sent to Mars in the framework of NASAs Mars2020.

iSTENT

Real Time Monitoring of Hemodinamic Variables using Smart Stents (iSTENT) based on Capacitive and Bioimpedance Sensors

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Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia, Innovación y Universidades**
Reference: **RTI2018-093512-B-C21**
Start date: 01/01/2019
End date: **31/12/2021**
Funding: **99.704,00 €**

The coordinated proposal Real Time Monitoring of Hemodinamic Variables Using Smart Stents (iSTENT) Based on Capacitive and Bioimpedance Sensors aims to progress towards the design and manufacture of microsystems for the real-time monitoring of Intra Stent Restenosis (ISR) and Heart Failure (HF) by means of measuring relevant parameters for the diagnosis of cardiovascular diseases. In short, collaborating to improve the life quality of patients, thanks to the advancement in eHealth, increasing the effectiveness of biomedical monitoring systems.

The SubProject 1 (SP1) Integrated Microsystem based on bioimpedance measurements for the monitoring of arterial restenosis, focuses its work hypothesis on the implementation of electrical bioimpedance measurements to obtain the required useful information of the stent that allows to evaluate the degree of the coronary artery obstruction where it is implanted, as well as the hemodynamic variables involved in its state. The SubProject 2 (SP2) Integrated heterogeneous system for the monitoring of heart failure based on capacitive pressure sensors, proposes to use capacitive MEMS pressure sensors for the monitoring of blood pressure and HF by means of the left ventricle preload. Thus, SP1 pursues the realization of an iStent with the ability to monitor its internal obstruction (ISR) once implanted, avoiding the invasive and high risk procedure for the patient that involves performing a catheterization. Similarly, SP2 proposes the design, characterization and manufacture of an iStent for the monitoring of the HF, based on an heterogeneous integrated circuit for the pressure measurement in the distal pulmonary artery without having to use invasive diagnostic techniques. Besides, both proposals target the adquisition of additional measurements of other hemodynamic variables.

ASICs-AVATART

High-Speed and High-Voltage ASICs for Extreme Radiation and Temperature Enviroments

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Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Ciencia, Innovación y Universidades**

Reference: **RTI2018-099825-B-C32**
Start date: 01/01/2019
End date: **31/12/2021**
Funding: **146.652,00 €**

This project (ASICs-AVATART) supposes a necessary and important technological activity of development of mixed signal ASICs for space applications. This activity was started in 2008 within the framework of the MetNet mission and resulted in the creation of a group at the Microelectronics Institute of Seville/University of Seville, which has since them specialized in this type of designs. Thanks to this effort, it has been possible to respond, for example, to the need arising within the framework of the aforementioned MEDA station (to condition the signal of its wind sensors) and the possibility of making recurrent systems more and more compact (less weight, volume, consumption, etc.) as the ASIC-SIS20 for solar irradiance sensors (InMars). It should be noted that IMSE/US has its own RHBD library in AMS 0.35µm technology, with designs that have been shown to operate at temperatures of -126°C, and that also has experience in designs for space with other technologies and libraries (IMEC-DARE in UMC 180 nm, SOI-XFAB).

It should be noted that the development of mixed-signal ASICs for space use is identified in H2020 as a strategic line for Europe and nondependence. This project aims to advance in the line of Integrated Circuits for radiation environments and with the particularity of very low temperatures. Specifically, the project focuses on High Voltage and High Speed cases. Although there are works in this regard, the particularity of the present project is that it is intended that the circuits work at very low temperatures without having to be heated to accommodate the operating situation to the typical industrial temperature ranges for which they are usually characterized. On the other hand, the high speed and / or high voltage features usually require different technologies, which is why this project seeks to integrate them into the same package by exploring the multi-die techniques. Of course, these techniques must also be adapted to operate at very low temperatures without the need for heating. In the end, this project aims to provide increasingly compact solutions that are equipped with added values such as reliability and re-usability.

StatSeT

Statistical approach to defect simulation in complex Analog and Mixed-Signal circuits: application to radiation-induced Single-Event Transients

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Projects Details:

Type: **Research project**
Funding Body: **Ministerio de Ciencia, Innovación y Universidades**
Reference: **RTI2018-098513-B-I00**
Start date: 01/01/2019
End date: **31/12/2021**
Funding: **75.141,00 €**

In salety-critical applications, detecting fabrication delects is of utmost importance, even if they do not impact significantly the performance. Defect-oriented test approaches are thus necessary, but their validation is cumbersome. Indeed, defect simulation is unavoidable but computationally demanding. For complex Analog and Mixed-Signal (AMS) circuits and systems, the number of defect candidates may be very large. If the evaluation of each defect candidate requires a complex transient simulation, exhaustive simulation is simply intractable. Sound statistical approaches to estimate defect coverage have been proposed, but one of the main shortcomings of these approaches is that of experimental validation. On one hand, it is almost impossible to get access to delect statistics of commercial parts since this data is a very sensitive in terms of company image. On the other hand, it is al so impossible to manulacture (and test) a sulficient amount of circuits to get reliable statístics in an academic environmenl. Europractice integration services usually give access to around 50 parts, very far of the production level necessary to estimate a defectivity rate in the arder of tens 01 ppm.

In order to tackle this validation issue, this project propases to adapt the framework of statistical assessment of defect coverage to the study of radiation-induced Single-Event Transient (SET) sensitivity in complex Analog and Mixed-Signal circuits.

HARDBLOCK

Hardware-based Security for Blockchain Technologies

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Projects Details:

Type: **Research project**
Funding Body: **Ministerio de Ciencia, Innovación y Universidades**
Reference: **RTC-20176595-7**
Start date: 2018
End date: **30/06/2021**
Funding: **175.170,00 €**

Objectives of the project:

- The main objective of HardBlock project is to develop a blockchain technology able to reduce the scalability problems of public blockchains.

- The new concepts of Proofs of Physical Existence and Proofs of Physical Presence will be exploited to reduce the highly maintenance costs of Proofs of Work.

- New hardware elements will be designed and implemented to support the Proofs of Physical Existence, providing the unique identification of things and avoiding tampering and counterfeiting.

- New hardware elements will be designed and implemented to support the Proofs of Physical Presence using biometrics. The objective is the user authentication with the highest authentication level (AAL3 according to NIST SP 800-63): using a compact and tamper-resistant device, under the control of the user, and with template protection.

- HardBlock will provide secure key exchange without using trusted third parties and avoiding man-in-the-middle attacks, and will exploit the use of post-quantum algorithms mainly based on lattice cryptography.

- The project will explore new application fields such as the combination of Internet of Things (IoT) with blockchain technologies.

HW-IDENTIoTY

Design of hardware solutions to manage people and things identities with trust, security, and privacy in IoT ecosystem

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Projects Details:

Type: **Research project**
Funding Body: **Ministerio de Ciencia, Innovación y Universidades**
Reference: **TEC2017-83557-R**
Start date: 2018
End date: **30/09/2021**
Funding: **139.150,00 €**

In the Internet of Things (IoT) ecosystem, people will be surrounded by a growing number of smart devices with sensors and actuators, which capture information about our environments and act upon them autonomously (our cities, homes, cars or bycicles and even our body). As a matter of fact, people already interact more with or through these devices instead of interacting directly. The IoT infraestructure is aimed at improving our quality of life, but if it is not trust, secure and does not guarantee our privacy, the consequences can be catastrophic.

A first challenging aspect is to ensure that individuals and devices are trusted and authentic and, hence, that their identities are resistant to impersonation and counterfeiting. Since the physical nature of an IoT device lies in the hardware it is made of, HW-IDENTIoTY project will design hardware solutions based on physical unclonable functions (PUFs) to generate inherent identities of devices. Since the unique features of a person can be captured by a biometric recognition system, HW-IDENTIoTY project will design hardware solutions to implement lightweight biometric recognition techniques that could be implemented in a wearable, so that the digital identity of the person is generated locally by a trusted device under the supervision of the identity owner.

A second critical issue is to guarantee privacy. For this purpose, the digital identities will be transformed in such a way that the resulting data cannot be attributed to a specific individual or device without the use of additional information. HW-IDENTIoTY project will design hardware solutions to implement Helper Data algorithms in the case of devices and template protection techniques in the case of individuals.

The third aspect addressed will be the design of hardware solutions robust against attacks to implement cryptographic primitives paradigm. They will be related to symmetric and lightweight cryptography in the case of wearables (with constrained resources and low-power consumption requirements) and to elliptic curve cryptography in the case of embedded systems. The availability of counterfeit-resistant identities will be exploited to address problems associated with digital chains of custody and traceability in IoT.

PULPOSS

Processing for Ultra Low POwer using Steep Slope devices: circuits and arquitectures

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Projects Details:

Type: **Research project**
Funding Body: **Ministerio de Ciencia, Innovación y Universidades**
Reference: **TEC2017-87052-P**
Start date: 2018
End date: **30/06/2021**
Funding: **85.910,00 €**

Different applications with a great social and economic impact (IoT, wearables, implantable devices, WSNs) demand circuits with very low power consumption and

efficient in terms of energy. In this context, the field-effect transistor has severe limitations associated with its SS, that cannot be reduced below 60mVIdec, which prevents it from reducing its polarization voltage, without significantly degrading its performance in terms of speed or excessively increasing its leakage curren!. Currently important efforts are devoted to the development of "steep slope" devices that do not exhibit this limitation. This project addresses the design of circuits and architectures implemented with these transistors in order to contribute to the development of such applications. The work developed in NACLUDE (TEC2013-40670-P) with tunneling transistors (TFETs) is extended to other steep slope devices, including negative capacitan ce transistors (NCFET, FeFET), transistors incorporating materials that exhibi! phase !ransitions (HyperFET, PC-FET) or "super steep slope" devices tha! combine these physical phenomena with TFETs (PC-TFET, NC-TFET) to improve their performance.

Although there is consensus in the scientific community about !he potential of these devices to implement circuits more efficient in terms of power consumption and energy than MaS and FinFET transistors, the simple replacement of conventional transistors by steep slope devices does not allow to obtain the maximum benefit of its use. It is necessary to adapt the topologies andlor architectures to the distinctive characteristics of ea eh device. The general objective of this project is the development of logical architectures and circuits with steep slope devices to optimize their performance in terms of power, energy or power-speed trade-offs in different application scenarios. The specific objectives that we formulate are: 1) To develop, analyze, validate and evaluate appropriate topologies for basic logical blocks; 2) to Develop, analyze, validate and evaluate appropriate logic architectures; 3) To apply design techniques for low power; 4) To explore alternative computing paradigms to CMOS logic; 5) To maintain a library of models of steep-slope devices updated with the advances and proposals that are taking place.

TOGETHER

Towards Trusted Low-Power Things: Devices, Circuits and Architectures

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Projects Details:
Type: **Research project**
Funding Body: **Ministerio de Economía, Industria y Competitividad**
Reference: **TEC2016-75151-C3-3-R**
Start date: 30/12/2016
End date: **29/06/2021**
Funding: **240.911,00 €**

To bridge the gap between the physical and digital worlds, any type of product would need to integrate networked electronic components and systems, built on micro/nanotechnologies, in what has been called "Internet of Things" (IoT). To fulfill the IoT vision, many technology enablers are required, with trusted (i.e., reliable and secure) as well as low-power ICs and components, among others, playing a pivotal role. All these enablers must be properly handled with a multidomain approach -covering device, circuit and architectural levels- in a context where technology scaling has slowed down. Thus, at technology level, innovations in materials and device structures will be required and, next to this, low-power robust circuits and alternative architectures will have to be implemented. Consequently, the experience of researchers with complementary expertise must be properly combined under a collaborative framework. Following these guidelines, device reliability engineers (UAB) and analog and digital circuit designers (IMSE and UPC) will work together in this project on the design of low-power, variability-resilient nanoelectronic circuits and systems, by using a multilevel approach and taking into account IoT challenges.

To achieve this general objective, several lines of work will be followed. Since circuit and system design for IoT relies upon a deep knowledge of phenomena at device level, a detailed statistical and multiscale characterization of the variability in advanced CMOS devices will be done in all regimes of operation, for the development of variability-aware compact models. Emerging devices (i.e., memristors and graphene-based devices) will be also considered to evaluate their suitability as building components in alternative circuits and architectures. At circuit and system levels, low-power and variability-resilient design strategies and methodologies will be developed. Variability will be tackled from two perspectives: palliation and exploitation. From a palliative perspective, adequate design methodologies will be created, able to consider and reduce variability across many hierarchical levels in a complex AMS/RF system. Also, the use of Body Bias modulation for variability mitigation in RF and digital circuits in FDSOI technologies will be analyzed. From the exploitation perspective, unreliability aspects in CMOS and memristive devices will be explored for the implementation of cryptographic primitives. Energy-efficient hierarchical design methodologies will be implemented to reduce power consumption in AMS/RF circuits and ultra-low voltage AMS/RF and digital circuits will be designed. Non-conventional strategies for computing systems and non-von Neumann computing architectures will be studied too. Finally, the adoption of emerging technologies for alternative computing architectures (combining memristors and FETs) as well as neuromorphic architectures will be addressed. The innovations in devices, design techniques, extremely low-power and reliable circuits and architectures will enable competitive advantages in numerous IoT applications and markets, supporting the relevance of the proposed research from the societal, industrial and economical points of view. This fact, together with the experience of the proposing partners, foresees publications and technology transfer of the results.

REGIONAL GOVERNMENT

VERSO

Vertical integration of image sensors with embedded parallelism.

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Projects Details:
Type: **Border Projects**
Financing body: **Junta de Andalucía**
Reference: Not available
Start date: 05/10/2021
End date: **31/05/2023**
Total granted: **78.700,00 €**

The demand for image sensors is unstoppable and their market share has grown exponentially over the last decade. In this environment of continuous demand, vertically integrated technologies are emerging as the technological vehicle through which image sensors will evolve in the future.

Vertical integration technologies allow greater processing capacity and memory to be incorporated within the same pixel, without affecting its size or the ratio between the area dedicated to light sensing and the total area of the pixel ('fill factor'). Furthermore, it is envisaged that several different technologies or variants of the same technology may co-exist and be applied to pixel design.

The project includes, in its initial phase, a feasibility study of modern vertical integration technologies with the company TELEDYNE-ANAFOCUS as preferred partner. In a later phase, the design of two image sensors that allow these objectives to be met and to demonstrate the viability of the technology by searching for novel pixel architectures that can exploit its potential will be addressed. The company will provide a detailed study on the electrical characteristics of a modern vertical integration technology, based on its previous experience. Specifically, it will detail the electrical characteristics of the available vertical interconnections. In parallel, the company will provide design specifications to be able to transfer the chips that are designed to the market. For the design of the sensors,

The sensors to be integrated will have two different image sensor architectures. The first of them is a sensor based on SPADs, capable of measuring the time of flight. The second is a high dynamic range sensor that combines asynchronous event-based operation with an output data format identical to that of APS sensors.

COGNITIO

Design of cognitive interfaces for IoT devices with artificial intelligence.

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Projects Details:
Type: **Challenges of Andalusian society**
Financing body: **Junta de Andalucía**
Reference: **P20_00599**
Start date: 05/10/2021 End date: **30/06/2023**
Total granted: **50.100,00 €**

The fundamental objective of this project is the design and development of methodologies for the design of cognitive analog-digital interfaces for a more efficient digital transformation. To do this, analysis, synthesis and design methods will be proposed from the system level to the physical level, with a greater degree of programmability, so that the specifications at each level of abstraction can be managed by Artificial Intelligence (AI) algorithms. based on neuromorphic processing. Although the project must take into account aspects of the entire communication system, the activity focuses on the analog-to-digital converter or ADC (for 'Analog-to-Digital Converter') as a fundamental building block of IoT devices. For the demonstration of the proposed techniques, two 28nm chip fabrication technologies will be considered:

The comparative study of these technological processes is part of the objectives of the project, in order to implement the circuits and systems that are proposed with the lowest possible energy consumption. Therefore, the research to be carried out aims to address one of the great challenges identified in PAIDI2020 and RIS3-Andalusia, such as 'Making Andalusia an integrated society in the digital world, through the incorporation of new telecommunications infrastructures... new ICT developments...', thanks to the development of enabling technologies such as digitization based on cognitive circuit techniques managed by artificial intelligence that are proposed in the project, and that will allow increasing the degree of interweaving of IoT devices in Andalusian society.

SYMAS

Measurement and electrostimulation system for cell differentiation and motility applications.

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Projects Details:
Type: **Research Project**
Funding Body: **Junta de Andalucía**
Reference: **P18-FR-2308**
Start date: 01/01/2020 End date: **31/12/2022**
Funding: **79.800,00 €**

It is proposed to carry out embedded Electronic Systems (ES) for the supervision and characterization of cells and cell cultures, which allow to act on them by means of programmable electrostimulation signals. The objective is to study, know and improve the techniques of cell differentiation towards different types of lineages and tissues of interest in regenerative medicine. The design and manufacture of systems with reduced weight and size, energy autonomous and wireless are pursued, which reduce the workload, automate experiments and monitor in real time the evolution of a cell culture based on the electrical BioImpedance (BI) as a marker. It is proposed to monitor the evolution of cell lines: neuroblastomas, myoblastomas and osteoblasts, useful in neuronal therapies and engineering of muscle and bone tissues, towards the conformation of the corresponding cell or tissue type, optimizing the differentiation processes through the adequate design of signals of electrical stimulation.

From the results obtained in a first measurement setup, two more setups are proposed: one oriented to the clinical development of tissue engineering; and another dedicated to the study and characterization at the cellular level of electrostimulation processes, through the manufacture of microelectrode arrays (MicroElectrode Array, MEA). Taking advantage of this last setup, cell motility experiments are proposed to determine the position and velocity of tumor cells (MCF7) in cultures, and their use in cancer studies. In summary, ES will be developed for monitoring and electrostimulation measuring electrical BIs, in parallel to a cell and tissue biometry procedure for the real-time identification of the biological material differentiated or not, and its dynamic characteristics: position, trajectory and speed. The results will be validated using biomedical experimentation standards in the proposed cell lines.

SPADARCH

Flexible SPAD-Based CMOS Chip Architectures for Time Correlated Single Photon Counting.

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Projects Details:
Type: **Transfer activities**
Funding Body: **Junta de Andalucía**
Reference: **US-1264940**
Start date: 01/02/2020 End date: **31/1/2022**
Funding: **90.000,00 €**

Based on previous academic and industrial activities of the TIC-179 group in CMOS Image Sensors (CIS) with conventional photo-diodes, the team has devised knowledge over the last few years regarding architectures, circuits, methods, chips and system demonstrators for image sensors based on Single Photon Avalanche Diodes (SPAD). This knowledge has resulted in prime line publications and patent proposals that have prompted interest for technology transfer. This project addresses challenges identified following detailed measurements of these previous sensors and cameras and which extend over different levels, namely:

• Electron Device Level. The target here is to improve the response of SPAD photosensors by using SILVACO´s Atlas TCAD (Technology Computer-Aided Design) tools for device engineering.

• Pixel Level. Targets here are related to the use of active circuitry to control avalanche currents.

• Sensor Architectural Level. Challenges here are mostly linked to the subsystems employed to measure and encode pieces of information of the scenes, namely TDCs for measuring arrival times and counters for counting photons.

• Post-Processing Level. Challenges here are related to the fact that SPAD measurements are of statistical nature. Either averages or histograms must be employed to extract relevant data. These statistical measurements require memory resources; for instance, some 1,000 inter-frames may be needed to obtain a single relevant frame.

• Application Level. This project targets enabling technologies that are transversal to many applications. Still, application requirements will be used as "beacons" for the R&D activities. Particularly, requirements set by solid-state LIDAR (LIght Detection And Ranging).

INFRAESTRUCTURA 5169

Establishment of a Technology Surveillance Service for Promotion and Commercialization of the Technologies Developed at the Institute of Microelectronics of Seville (IMSE-CNM)

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Projects Details:
Type: Facilities
Funding Body: Junta de Andalucía
Reference: 5169
Start date: 01/02/2020
End date: 30/06/2022
Funding: **64.647,53 €**

The common objective of the actions carried out in this project is to increase the transfer to industry and society of the results of the research developed at the Institute of Microelectronics of Seville for the improvement of processes and products and for the development of specific applications. To this end, the creation of a Projects and Transfer Unit with specific tasks of prospecting, dissemination, support and promotion of transfer activities is planned.

The launch of this initiative reflects two motivations of different nature. On the one hand, it seeks to increase the return on investments and guarantee the transfer of results generated in the Institute, augment its visibility in the industrial sector, promote the use of its infrastructures by external research groups, and intensify participation in research and development programs focused on collaboration between public and private entities. On the other hand, the center aims to fulfill its function as Agent of the Andalusian Knowledge System specialized in the area of Microelectronics, making available to Andalusian companies the services and technologies necessary for the development of innovative products.

NEURO-RADIO

Cognitive radio embedded with neural learning.

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Projects Details:
Type: **Research Project**
Funding Body: **Junta de Andalucía**
Reference: **US-1260118**
Start date: 01/02/2020 End date: **31/1/2022**
Funding: **30.000,00 €**

The paradigm known as the Internet of Things or IoT refers to the interconnection ofbillions of devices autonomously and capable of interacting with both your own environment as well as with the network intelligently. One of the main bottleneckshat we currently find ourselves within this model is given by the limitation of the communication systems when sharing the electromagnetic spectrum between an increasingly greater number of devices supporting huge volumes of information. Another of the great challenges of the IoT is based on the need to reduce the power consumption of devices to maximize their autonomy. Cognitive radio technology proposes to make efficient use of the spectrum by dynamically modifying the transmission parameters in based on information sensed from the environment. This proposal requires, on the one hand, to design a communications system where digitization moves to the antenna (both in the emitter and receiver) to allow adaptation and configurability through software, and on the other hand, to design a computer system capable of dynamically selecting the most suitable parameters for the communications system depending on the conditions of the environment, all while minimizing power consumption.
In this project, we propose the design of a cognitive radio system that combines adaptive signal processing and digitizing techniques in conjunction with a processor neuromorphic system that modifies the parameters of the system through machine learning to 5G communication systems. For the neuromorphic processor, we propose the use of networks Binary neurons based on memristive nano-devices. These emerging devices allow their resistance to be modified depending on the values of voltage or current applied, emulating the synaptic connections of the brain that modify their value depending on the stimuli, providing learning capacity. With these devices, we can implement architectures that simultaneously carry out online learning and high-speed processing with low power consumption.

CRYPTOHARDWEAR

Hardware solutions to face the new cryptographic challenges of wearable devices.

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Projects Details:
Type: **Research project**
Funding Body: **Junta de Andalucía**
Reference: **US-1265146**
Start date: 01/02/2020 End date: **31/1/2022**
Funding: **89.950,00 €**

Wearable devices are characterized by being light, small and comfortable to wear. They are used in health-related applications (medical devices that monitor the activity of the heart, breathing, blood glucose level,...), activities daily (distance traveled, speed, calories consumed, ...), virtual reality (microcameras or glasses that retransmit images or video), or work (access control, presence, payments or transaction authorization, ...). Security is essential in these devices because represent the digital origin of the information, which in many cases is sensitive, and to protect information must resort to cryptographic techniques.

A critical element of contemporary cryptography is the generation and correct management of digital identities that intervene in the production or transformation of information, of way that guarantees not only security but also trust and privacy. In the case of identities of people, which are recognized by biometrics, a critical element is to protect characteristics (templates) that represent individuals and eliminate their traceability. In the context of wearable devices, another critical element is that the new solutions cryptographic ones that arise (for example those that are called post-quantum) can be implemented on hardware platforms with reducEd computational capabilities, memory, communication and power consumption.
The CryptoHardWear project will look at the fundamentals of two types of cryptography relatively recent: identity-based cryptography and identity-based cryptography. learning problems with errors (which is post-quantum) to, on the one hand, explore the two feasibility and effectiveness of digital hardware solutions that allow the implementation of these techniques in wearables and, on the other hand, explore the advantages that these techniques can involve extracting the identities of the devices from the wearable itself (through functions physically unclonable or PUFs of your hardware) and the identities of the users (via biometrics), both extracted with an inevitable distribution of errors.

TRANSFERENCIA CONOCIMIENTO

Microelectronic knowledge and technology transfer about multi-modal crypto-biometrics

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Projects Details
Type: **Transfer activities**
Funding Body: **Junta de Andalucía**
Reference: 5926
Start date: 01/02/2020
End date: **31/01/2021**
Funding: **38.015,00 €**

This project aims to increase the knowledge and microelectronic technology transfer about multi-modal crypto-biometrics among the applicant research group, which belongs to the PAIDI TIC-180 research group Design of Digital and Mixed Integrated Circuits and carries out its research in the Microelectronic Institute of Seville (IMSE-CNM, joint center of the University of Seville and CSIC), and the Andalusian productive sector, with a clear international projection. For this, the activities of the project will include: (a) conducting a market study and technological surveillance, (b) studying the product orientations that can have the most demand in the market, (c) selecting the crypto-biometric modalities to meet the specifications of the market, (d) developing prototypes and proofs of concept, and (e) promote the technology.

CEI

Sensores de imagen y vision con integracion vertical para aplicaciones de inteligencia artificial

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Projects Details
Type: **Research project**
Funding Body: **Junta de Andalucía**
Reference: **CEI-7-TIC-179**
Start date: 27/12/2019
End date: **27/12/2021**
Funding: **50.296,40 €**

I+D+i en arquitecturas de sensores de imagen y visión con tecnologías de integración vertical para afrontar los retos de la IA en sectores TIC. Con el objetivo final de desplegar sensores de visión miniaturizados, de altas prestaciones y mínimo consumo, en el mayor número de sistemas, con énfasis en: IoT, Automoción, Robótica.
En concreto, se consideran tres arquitecturas: a) una basada en SPADs para medición del tiempo de vuelo; b) una de alto rango dinámico que combina operación basada en eventos con formato de datos de salida de los APS estándar; c) una de bajo ruido y alta veocidad.

OFICINA PROYECTO

Implantación de un servicio de vigilancia tecnológica para la promoción y comercialización de las tecnologías desarrolladas en el Instituto de Microelectrónica de Sevilla (IMSE-CNM)

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Projects Details
Type: **Transfer activities**
Funding Body: **Junta de Andalucía**
Reference: **5877**
Start date: 01/11/2019
End date: **30/04/2021**
Funding: **54.466,67 €**

El objetivo común de las actuaciones para las que se solicita esta ayuda es aumentar la transferencia a la industria y a la sociedad de los resultados de la investigación desarrollada en el Instituto de Microelectrónica de Sevilla, como base para la mejora de procesos y productos y para el desarrollo de aplicaciones específicas. Para ello se planea la creación de una Unidad de Proyectos y Transferencia con tareas específicas de prospección, difusión, apoyo y fomento de actividades de transferencia.
La puesta en marcha de esta iniciativa obedece a dos motivaciones de distinta naturaleza. Por una parte, se persigue incrementar el retorno de las inversiones y garantizar la transferencia de resultados generados en el Instituto, aumentar su visibilidad en el sector industrial y promover el uso de sus infraestructuras por grupos de investigación externos, así como intensificar la participación en programas de investigación y desarrollo enfocados a la colaboración entre entidades públicas y privadas. Por otra, el centro pretende cumplir su función como Agente del Sistema Andaluz del Conocimiento especializado en el área de la Microelectrónica, poniendo a disposición de las empresas andaluzas los servicios y tecnologías necesarios para el desarrollo de productos innovadores.

EU PROJECTS

SPIRS

Secure Platform for ICT Systems Rooted at the Silicon Manufacturing Process.

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Projects Details:
Type: **Research project**
Funding Body: **European Union**
Reference: **952622**
Start date: 01/10/2021 End date: **30/09/2024**
Funding: **610.028,25 €**

Our society is continuously demanding more and more intelligent devices, along with network infrastructures and distributed services that make our daily lives more comfortably. However, the frantic adoption of Internet of Things (IoT) technologies has led to widespread implementations without a deep analysis about security matters.

This project encompasses the complete design of a platform, so-called SPIRS platform, which integrates a hardware dedicated Root of Trust (RoT) and a processor core with the capability of offering a full suite of security services. Furthermore, the SPIRS platform will be able to leverage this capability to support privacy-respectful attestation mechanisms and enable trusted communication channels across 5G infrastructures.

RoT is implemented in hardware with a dedicated circuitry to extract a unique digital identifier for the SPIRS platform during its entire lifetime. To build a complete solution, the project also features a Trusted Execution Environment (TEE), secure boot, and runtime integrity. Furthermore, resilience and privacy protection are major concerns in this project, and it endeavors to the design of a decentralized trust management framework targeted to minimize the impact of Single Point of Failure (SPOF) risks and achieve adequate security and privacy tradeoffs. To facilitate the tasks of validation and testing, SPIRS platform is conceived as an open platform that can easily integrate other building blocks and facilities upgrades.

The project goes beyond the construction of the SPIRS platform and it provides solutions to integrate it in the deployment of cryptographic protocols and network infrastructures in a trustworthy way, leveraging the RoT provided by the platform.

To validate SPIRS results, the project considers two different scenarios: Industry 4.0 and 5G Technologies.

SPINAGE

Weighted Spintronic-Nano-Oscillator-based Neuromorphic Computing System Assisted by laser for Cognitive Computing

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Projects Details:
Type: **Research Project**
Funding Body: **European Union**
Reference: **H2020-FETOPEN-2020-01-899559**
Start date: 01/09/2020 End date: **31/08/2024**
Funding: **437.577,00 €**

The brain is a highly complex, high performance and low energy computing system due to its massive parallelism and intertwined network, which outperforms the current computers by orders of magnitudes, especially for cognitive computing applications. A large effort has been made into understanding the computing and mimicking the brain into an artificial implementation, so-called neuromorphic computing that has received much attention thanks to the advances in novel nanoscale technologies.

The current implementation of the neuromorphic computing systems (NCS) using Complementary Metal-Oxide-Semiconductor (CMOS) technologies has 5-6 orders of magnitude lower performance (operation/sec/Watt/cm3) compared to the brain. Spintronic devices, using the spin of the electron instead of its charge, have been considered one of the most promising approaches for

implementing not only memories but also NCSs leading to a high density, high speed, and energyefficiency. The main goal of SpinAge is to realize a novel NCS enabling large-scale development of braininspired devices outclassing the performance of current computing machines.

This will be achieved by the novel structures using spintronics and memristors, on-chip laser technology, nano electronics and finally advanced integration of all these technologies. We expect this unprecedented combination of emerging technologies will lead to at least 4-5 orders of magnitude better performance than the state-of-the-art CMOS-based NCSs. The approach taken in SpinAge is to implement synaptic neurons using novel nanoscale weighted spin-based nanooscillators, assisted by a low-energy laser pulse irradiation from an integrated plasmonic laser chip, integrated all with the CMOS interfacing electronics for a proof-of-concept of a 16x16 NCS for cognitive computing applications. Our breakthrough platform technology will demonstrate EU leadership of advanced neuromorphic computing.

APPROVIS3D

Analog PROcessing of bioinspired VIsion Sensors for 3D reconstruction

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Projects Details:
Type: **Research project**
Funding Body: **European Union**
Reference: **CHIST-ERA 2018-ACAI, Ref: PCI2019-111826-2**
Start date: 01/04/2020
End date: **31/03/2023**
Funding: **149.772,00 €**

APROVIS3D project targets analog computing for artificial intelligence in the form of Spiking Neural Networks (SNNs) on a mixed analog and digital architecture. The project includes including field programmable analog array (FPAA) and SpiNNaker applied to a stereopsis system dedicated to coastal surveillance using an aerial robot. Computer vision systems widely rely on artificial intelligence and especially neural network based machine learning, which recently gained huge visibility. The training stage for deep convolutional neural networks is both time and energy consuming. In contrast, the human brain has the ability to perform visual tasks with unrivalled computational and energy efficiency. It is believed that one major factor of this efficiency is the fact that information is vastly represented by short pulses (spikes) at analog -not discrete-times. However, computer vision algorithms using such representation still lack in practice, and its high potential is largely underexploited. Inspired from biology, the project addresses the scientific question of developing a lowpower, end-to-end analog sensing and processing architecture of 3D visual scenes, running on analog devices, without a central clock and aims to validate them in real-life situations. More specifically, the project will develop new paradigms for biologically inspired vision, from sensing to processing, in order to help machines such as Unmanned Autonomous Vehicles (UAV), autonomous vehicles, or robots gain high-level understanding from visual scenes.

The ambitious long-term vision of the project is to develop the next generation AI paradigm that will eventually compete with deep learning. We believe that neuromorphic computing, mainly studied in EU countries, will be a key technology in the next decade. It is therefore both a scientific and strategic challenge for the EU to foster this technological breakthrough. The consortium from four EU countries offers a unique combination of expertise that the project requires. SNNs specialists from various fields, such as visual sensors (IMSE, Spain), neural network architecture and computer vision (Uni. of Lille, France) and computational neuroscience (INT, France) will team up with robotics and automatic control specialists (NTUA, Greece), and low power integrated systems designers (ETHZ, Switzerland) to help geoinformatics researchers (UNIWA, Greece) build a demonstrator UAV for coastal surveillance (TRL5).

Adding up to the shared interest regarding analog based computing and computer vision, all team members have a lot to offer given their different and complementary points of view and expertise. Key challenges of this project will be end-to-end analog system design (from sensing to AIbased control of the UAV and 3D coastal volumetric reconstruction), energy efficiency, and practical usability in real conditions. We aim to show that such a bioinspired analog design will bring large benefits in terms of power efficiency, adaptability and efficiency needed to make coastal surveillance with UAVs practical and more efficient than digital approaches.

MEM-SCALES

Memory technologies with multi-scale time constants for neuromorphic architectures.

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Projects Details:
Type: **Research project**
Funding Body: **European Union**
Reference: **H2020-ICT-2019-2-871371**
Start date: **01/01/2020 End date: 31/12/2022**
Funding: **569.926,00 €**

The project MeM-Scales aims at lifting neuromorphic computing in analog spiking microprocessors to an entirely new level of performance. Work in this project is based on a dedicated commitment that novel hardware and novel computational concepts must be co-evolved in a close interaction between nano-electronic device engineering, circuit and microprocessor design, fabrication technology and computing science (machine learning and nonlinear modeling). A key to reflecting 'hardware physics' in 'computational function' and vice versa is the fundamental role played by multiple timescales. Here MeM-Scales introduces a number of innovations. On the side of physical substrates, novel memory and device technologies, supporting on-chip learning over multiple timescales for both synapses and neurons, will be fabricated. To enable timescales spanning up to 9 (!) orders of magnitude both volatile memory and non-volatile memory as well as Thin Film Transistor technology will be exploited. On the side of computational theory, autonomous learning algorithms and architectures supporting computation over these wide range of timescales will be developed. These computational methods are specifically tailored to cope with the low numerical precision, parameter drift, stochasticity, and device mismatch which are inherent in analog nano-scale devices.

These cross-disciplinary efforts will lead to the fabrication of an innovative hardware/ software platform as a basis for future products which combine extreme power efficiency with robust cognitive computing capabilities. This new kind of computing technology will open new perspectives, for instance, for high-dimensional distributed environmental monitoring, implantable medical diagnostic microchips, wearable electronics or human-computer interfacing.

NEURONN

Two-Dimensional Oscillatory Neural Networks for Energy Efficent Neuromorphic computing.

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Projects Details:
Type: **Research project**
Funding Body: **European Union**
Reference: **H2020-ICT-2019-2-871501**
Start date: **01/01/2020 End date: 31/12/2022**
Funding: **589.440,00 €**

Neuro-inspired computing architectures are one of the leading candidates to solve complex and largescale associative learning problems for AI applications. The two key building blocks for neuromorphic computing are the neuron and the synapse, which form the distributed computing and memory units. In the NeurONN project, we are proposing a novel neuroinspired computing architecture where information is encoded in the 'phase' of coupled oscillating neurons or oscillatory neural networks (ONN). Specifically, VO2 metal-insulator transition (MIT) devices and 2D memristors will be developed as neurons and synapses for hardware implementations. We predict VO2 MIT devices are up to 250X more energy efficient than state of the art digital CMOS based oscillators, where 2D memristors are up to 330X more energy efficient than state of the art TiO2 memristors. Moreover, the predicted energy efficiency gain of ONN architecture vs state of the art spiking neural network (SNN) architecture is up to 40X. Thus, NeurONN will showcase a novel and alternative energy efficient neuromorphic computing paradigm based on energy efficient devices and architectures.

Such ONN will demonstrate synchronization and coupling dynamics for establishing collective learning behavior, in addition to desirable characteristics such as scaling, ultralow power computation, and high computing performance. NeurONN aims to develop the first-ever ONN hardware platform (targeting two demonstrators) and complete with an ONN design methodology toolbox covering aspects from ONN architecture design to algorithms in order to facilitate adoption, testing and experimentation of ONN demonstrator chips by all potential users to unleash the potential of ONN technology.

HERMES

Hybrid Enhanced Regenerative Medicine Systems.

PI: **Bernabé Linares Barranco**
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Projects Details:
Type: **Research project**
Funding Body: **European Union**
Reference: **H2020-FET-PROACT-2018-01-824164**
Start date: 2019/ End date: **2023**
Funding: **438.511,25 €**

Brain disorders are the most invalidating condition, exceeding HIV, cancer and heart ischemia, with significant impact on society and public health. Regenerative medicine is a promising branch of health science that aims at restoring brain function by rebuilding brain tissue. However, repairing the brain is one of the hardest challenges and we are still unable to effectively rebuild brain matter. Epilepsy is particularly challenging due to its dynamic nature caused by the relentless brain damage and aberrant rearrangements of brain rewiring. To overcome the biological uncertainty of canonical regenerative approaches, we propose an innovative

solution based on intelligent biohybrids, made by the symbiotic integration of bioengineered brain tissue, neuromorphic microelectronics and artificial intelligence, to effectively drive self-repair of dysfunctional brain circuits and we validate it against animal models of epilepsy. HERMES fosters the emergence of a novel biomedical paradigm, rooted in the use of biohybrid neuronics (neural electronics), which we name enhanced regenerative medicine. To this end, HERMES will promote interdisciplinary cross-fertilization within and outside the consortium; it will extend the concepts of enhanced brain regeneration to philosophy, ethics, policy and society to foster the emergence of a new innovation eco-system. Intelligent biohybrids will represent a major breakthrough to advance brain repair research beyond regenerative medicine and neurotechnology alone; it will bring new knowledge in neurobiology, cognitive neuroscience and philosophy, and new neuromorphic technology and AI algorithms. HERMES will bring a giant conceptual leap that will shift the concept of biomedical interventions from treating to healing. In turn, it will potentially generate major returns on health care and society at large by bringing previously unimaginable possibilities to defeat disorders that represent today a global major burden of disease.

ACHIEVE

Advanced Hardware/Software Components for Integrated/Embedded Vision Systems

PI: **Ricardo Carmona Galán**
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Projects Details
Type: **Research project**
Funding Body: **European Union**
Reference: **765866**
Start date: 01/10/2017
End date: **30/09/2021**
Funding: **2.230.856,64 €**

ACHIEVE-ETN aims at training a new generation of scientists through a research programme on highly integrated hardware-software components for the implementation of ultra-efficient embedded vision systems as the basis for innovative distributed vision applications. They will develop core skills in multiple disciplines, from image sensor design to distributed vision algorithms, and at the same time they will share the multidisciplinary background that is necessary to understand complex problems in information-intensive vision-enabled aplliccations.

Concurrently, they will develop a set of transferable skills to promote their ability to cast their research results into new products and services, as well as to boost their career solutions for emerging technology markets in Europe and worldwide but also to drive new businesses through engaging in related entrepreneurial activities. The consortium is composed of 6 academic and 1 insdustrial beneficiaries and 4 industrial partners. The training of the 9 ESRs will be achieved by the proper combination of excellent research, secondments with industry, specific courses on core and transferable skills, and academic-industrial workshops and networking events, all in compliance with the call's objectives of international, intersectoral and interdisciplinary mobility.

CSIC PROJECTS

I-COOP+ 2019

Advanced Training in Digital System Design Techniques as a Basis for Promoting Innovation and Technological Development in Cuban Society

PI: **Santiago Sánchez Solano**
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Projects Details
Type: **Research project**
Funding Body: **CSIC**
Reference: **COOPB20420**
Start date: 01/01/2020
End date: **31/12/2021**
Funding: **23.958,00 €**

Continuous advances in microelectronic technologies have led to the development of reconfigurable hardware devices (FPGAs) that provide an increasing variety of resources for the implementation of complex digital systems, including those that incorporate powerful processing systems to facilitate the realization of embedded systems combining hardware and software elements on a single programmable chip (SoPC). The design of this type of system is key for the development of the applications and services that sustain the modern Digital Society, which is why it currently enjoys wide international relevance. Concurrently, in recent years have also appeared new methodologies and design environments based on the use of high-level synthesis tools (HLS) and hardware/software co-design techniques (SDSoC) that allow carrying out the processes of description, simulation and implementation of complex digital systems with a level of abstraction much higher than the previous ones, greatly increasing the productivity of designers and promoting the development of innovation projects.

The main objective of the proposed action is the training of Cuban university professors and researchers in the new of digital systems design techniques based on reconfigurable hardware devices (FPGA and SoC FPGA), as well as the incorporation of their teaching in master's and doctorate programs with electronic profile of Cuban universities in order to promote its use in the development of various R&D&I projects that benefit from its introduction. The strengthening of the scientific-technical capacities of Cuban research groups for the design and development of embedded digital systems on reconfigurable devices will provide, as main advantages, the reduction of their technological dependence and the increase of innovation activities in basic infrastructures and production systems, favoring the economic growth of the country.

i-LINK 2019

Advancing in cybersecurity technologies

PI: **Piedad Brox Jiménez** brox@imse-cnm.csic.es

Projects Details
Type: **Research project**
Funding Body: **CSIC**
Reference: **LINKA20216**
Start date: 01/01/2020
End date: **21/12/2021**
Funding: **23.738,00 €**

In current digitalized socities, cybersecurity is crucial to protect and preserve the growing social and economic benefits of Information Communication Technlology (ICT) systems. The rapid implantation and proliferation of these systems, as well as society´s overwhelming reliance on them, has exposed its fragility and vulnerabilities against attacks. New solutions of cyber-defense require multidisciplinary research groups that analyze hardware, software, networks and data security, not as isolated elements, but taking into account that they interrelate with each other and, therefore, trusted chains must be provided for the entire system.

The main objective of this proposal is to develop, deploy and integrate novel cybersecurity technologies that ensure the integrity, resilience and reliability of ICT systems. To achieve this goal, the consortium integrates three complementary research teams specialized in network and software security (University of Tampere, Finland), system security (University of Michigan, USA), and cryptography and hardware security (CSIC). This project encourages the collaboration by means of the participation in seminars that promote the exchange of ideas, medium-term stays of researchers to validate the proposed techniques, and the definition of a strategic plan to hold this collaboration over time submitting project proposals to international competitive calls, as well as analyzing agreements with foreign institutions involved in this project to facilitate collaboration.

INTRAMURAL SpaceD&T

Design and testing of mixed circuits for space applications.

PI: **Gildas Leger**

Projects Details:
Type: **Research project Funding**
Body: **CSIC**
Reference: **201950E040**
Start date: 01/05/2019 End date: **31/12/2023**
Funding: **105.958,77 €**

In this project, we propose to address the design and testing of analogue and mixed-signal circuits for space applications.

The technological evolution of CMOS technologies towards lower and lower dimensions has specific consequences in the field of space applications: the effects related to the total dose decrease with the scaling of the gate oxide, but on the other hand, the transient effects (known as singleevent effects, SEE) become more important as the capacities associated to the nodes decrease and therefore the amount of charge required to alter their voltage decreases.
In order to be able to tackle a design task with a certain degree of certainty, the first step is to be able to assess the impact of the different actions. It is therefore necessary to be able to calculate or simulate the effect of the SEEs on a circuit. This can be considered as solved since several papers show that the double-exponential current injection model at the body-source and body-drain junctions of CMOS transistors adequately reproduces the experimentally observed behaviour. However, for a circuit of a certain complexity, the number of charge injection sites is too large to allow a comprehensive simulation.

PUBLICATIONS

BOOKS | JOURNAL PAPERS | CONFERENCE PAPERS

BOOKS

White Paper 11: Artificial Intelligence, Robotics and Data Science

J.E. Marco de Lucas, M.V. Moreno-Arribas, S. Degli-Esposti, C. Sierra, F. Manyà, A. Colomé, N. Osman, D. López, J. Ramasco, L. Lloret-Iglesias, G. Alenyà, J. Villagrá, M.D. del Castillo, M. Schorlemmer, P. Noriega, T. Ausín, T. Serrano, A. Oyanguren, D. Arroyo-Guardeño and P. Brox

Libros Blancos. Desafíos Científicos 2030 del CSIC, 198 p, 2021
CSIC
ISBN: 978-84-00-10758-1

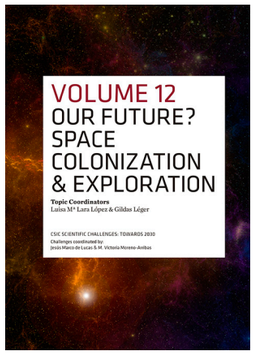
CSIC white paper on Artificial Intelligence, Robotics and Data Science sketches a preliminary roadmap for addressing current R&D challenges associated with automated and autonomous machines. More than 50 research challenges investigated all over Spain by more than 150 experts within CSIC are presented in eight chapters. Chapter One introduces key concepts and tackles the issue of the integration of knowledge (representation), reasoning and learning in the design of artificial entities. Chapter Two analyses challenges associated with the development of theories -and supporting technologies- for modelling the behaviour of autonomous agents. Specifically, it pays attention to the interplay between elements at micro level (individual autonomous agent interactions) with the macro world (the properties we seek in large and complex societies). While Chapter Three discusses the variety of data science applications currently used in all fields of science, paying particular attention to Machine Learning (ML) techniques, Chapter Four presents current development in various areas of robotics. Chapter Five explores the challenges associated with computational cognitive models. Chapter Six pays attention to the ethical, legal, economic and social challenges coming alongside the development of smart systems. Chapter Seven engages with the problem of the environmental sustainability of deploying intelligent systems at large scale. Finally, Chapter Eight deals with the complexity of ensuring the security, safety, resilience and privacy-protection of smart systems against cyber threats.

White Paper 12: Our future? Space colonization & exploration

J. Marco de Lucas, M.V. Moreno-Arribas, L.M. Lara, G. Leger, R. Duffard, I. González Gómez, O. Prieto Ballesteros, J. Ceballos Cáceres, B. Funke, D. Altadill, R. Benavides, J. Medina, G. Anglada-Escudé, M.J. Jurado, P. Godignon and G. Liñán

Libros Blancos. Desafíos Científicos 2030 del CSIC, 160 p, 2021
CSIC
ISBN: 978-84-00-10760-4

The exploration and colonization of the outer space represents a foreseeable future for the Humanity. This endeavour involves deepening our knowledge about the formation and evolution of the solar system, of other planetary systems, emergence of life (and its prospects once it exists), the interaction between Earth and Space (particularly with its Sun) and the impact of space conditions (radiation, gravity, etc.) on Earth-borne organisms. Materialization of this exploration and colonization currently drives technological developments in several fronts as optics, electronics and sensors just to mention a few. Other aspects as well law & ethics, psychology, biology, etc., cannot be discarded.



White Paper 14: Dynamic Earth: probing the past, preparing for the future

J. Marco de Lucas, V. Moreno-Arribas, C.J. Garrido, P. Gonzalez, F. Tornos, R. Carbonell, A. Geyer, M. García, A. Moreno, S. Giralt, M. Viana, F. Gallart, M.G. Llorens, D. García-Castellanos, J. García Guinea, M. Charco, J. Martí, J.J. Álvaro Blasco, M. Álvarez de Buergo, J. Álvarez Marrón, C. Ayala Galán, R. Amils, D. Brown, A. Castro Dorado, J. Ceballos Cáceres, J.M. Cebriá Gómez, A. Delgado Huertas, J. Fernández Torrres, R. Fort González, P. González-Sampériz, J. Huertas Puerta, A. Jiménez Díaz, F. Jiménez Espejo, J. López Gómez, T. Moreno, A. Negredo Moreno, J. Olof Ormö, O. Prieto Ballesteros, X. Querol, C. Rodrígez Ranero, M. Schimmel, V. Sellarés, J.M. Soler, J. Trigo Rodríguez and B. Valero Garcés

Book · Libros Blancos. Desafíos Científicos 2030 del CSIC, 111 p, 2021
CSIC
ISBN: 978-84-00-10764-2

Every day human activities involve interaction with our planet Earth. Everything around us is built upon the Earth, grows on the Earth, or depends on the environments and internal dynamics of the Earth to some degree. Indeed, Earth, s dynamic processes have strong influence on our society today as they have had at any time in human history, providing both major opportunities as well as challenges. Therefore, the knowledge about the Earth is the key to develop an informed citizenry and a global awareness of a common Planet and a common future. For example, dynamic processes during interaction between the tectonic plates that make up the outer 'skin' of Earth provide us with the valuable mineral deposits we need to develop our society, or the arable land and fertile soils needed to sustain it. Likewise, plate boundaries are the locus of hazards such as earthquakes, tsunamis, and volcanic eruptions that can cause large-scale disruption to, and displacement of, communities and economies. Just as one example, the March 11th, 2011 Tohoku earthquake offshore Japan, shows how a single-event natural disaster caused by one of the dynamic processes of the Earth (plate subduction) can have important socio-economic impacts that range from large-scale infrastructure damage to local and regional population relocation. Understanding the full range of Earth, s dynamic processes will not stop natural disasters like the Tohoku earthquake, but it will provide important information for developing models for their mitigation.

JOURNAL PAPERS

Módulo de inferencia difuso con base de conocimientos variable sobre hardware reconfigurable
A.J. Cabrera-Sarmiento, S. Sánchez-Solano and Y. García-Guirola

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A Mobile Platform for Movement Tracking based on a Fast-Execution-Time Optical-Flow Algorithm
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Neutron-Induced, Single-Event Effects on Neuromorphic Event-Based Vision Sensor: A First Step and Tools to Space Applications
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Insights into the Dynamics of Coupled VO2 Oscillators for ONNs
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Design of High-Efficiency SPADs for LiDAR Applications in 110nm CIS Technology
I. Vornicu, J.M. López-Martínez, F.N. Bandi, R. Carmona-Galán and A. Rodríguez-Vázquez

IEEE Sensors Journal, vol. 21, no. 4, pp 4776-4785, 2021
IEEE ISSN: 1530-437X

A Low-Resources TDC for Multi-Channel Direct ToF Readout based on a 28-nm FPGA
M. Parsakordasiabi, I. Vornicu, A. Rodríguez-Vázquez and R. Carmona-Galán

Sensors, vol. 21, no. 1, article 308, 2021
MDPI ISSN: 1424-8220

Editorial: A Year Ahead Full of New Initiatives
J.M. de la Rosa

IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 1, pp 4-4, 2021
IEEE ISSN: 1549-7747

Design of Wideband Comb Compensator based on Magnitude Response using Two Sinusoidals and Particle Swarm Optimization
G.J. Dolecek and J.M.de la Rosa

AEU - International Journal of Electronics and Communications, vol. 130, article 153570, 2021
ELSEVIER ISSN: 1434-8411

An efficient transformer modeling approach for mm-wave circuit design
F. Passos, E. Roca, J. Sieiro, R. Castro-Lopez and F.V. Fernandez

AEU - International Journal of Electronics and Communications, vol. 128, article 153496, 2021
ELSEVIER ISSN: 1434-8411

CONFERENCE PAPERS

Exploiting Correlation in Stochastic Computing based Deep Neural Networks
C.F. Frasser, P. Linares-Serrano, A. Moran, J. Font-Rossello, V. Canals, M. Roca, T. Serrano-Gotarredona and J.L. Rossello

Conference on Design of Circuits and Integrated Systems DCIS 2021
Visual and Acoustic Inference on Low-Cost IoT Systems
J. Fernández-Berni

Midterm Summer School MENELAOS 2021
The Two-Faced Variability Challenge in Nanoelectronics: Mitigation and Exploitation... and How to Get There
R. Castro-López

International Conference on Electrical and Electronics Engineering ELECO 2021
SoPC Implementation of a Genetic Algorithm for Circle Detection
L.F. Rojas-Muñoz, S. Sánchez-Solano, C.H. García-Capulín and H. Rostro-González

IEEE International Autumn Meeting on Power, Electronics and Computing ROPEC 2021
Pixel Circuitry for HDR and Tone Mapping vs. Digital Tone-Mapping Operators
J. Fernández-Berni

Huawei Workshop on Future Technologies for ISP 2021
Implementación en SoC de un Sistema Embebido para la Detección de Círculos en Imágenes Digitales
Luis F. Rojas-Muñoz, S. Sánchez-Solano, C.H. García-Capulín and H. Rostro-González

Congreso Internacional de Investigación Academia Journals Celaya CELAYA 2021
FeFETs for Phase Encoded Oscillatory based Computing
J. Nunez, M. Jimenez and M.J. Avedillo

Conference on Design of Circuits and Integrated Systems DCIS 2021
Modeling Edema Evolution with Electrical Bioimpedance: Application to Heart Failure Patients
M. Puertas, L. Giménez, A. Pérez, S.F. Scagliusi, P. Pérez, A. Olmo, G. Huertas, J. Medrano and A. Yúfera

Conference on Design of Circuits and Integrated Systems DCIS 2021
High-Level Inference On-Chip Enabled by Compressed Sensing
A. Khan, J. Fernández-Berni and R. Carmona-Galán

Conference on Design of Circuits and Integrated Systems DCIS 2021
Design Flow to Evaluate the Performance of Ring Oscillator PUFs on FPGAs
M.C. Martínez-Rodríguez, E. Camacho-Ruiz, S.

Sánchez-Solano and P. Brox

Conference on Design of Circuits and Integrated Systems DCIS 2021
A Reduced-scale Cortical Network with Izhikevich's Neurons on SpiNNaker
C. Chiplunkar, N. Gautam, I. Mediratta,A. Gait, S. Thomas, A. Rowley, T. Serrano-Gotarredona and B. Sen-Bhattacharya

IEEE International Joint Conference on Neural Networks IJCNN 2021
Design of Readout Channels for Direct-ToF LiDAR
M. Parsakordasiabi, A. Rodríguez-Vázquez and R. Carmona-Galán

Conference on Design of Circuits and Integrated Systems DCIS 2021
Baseline Features Extraction from Microelectrode Array Recordings in an in vitro model of Acute Seizures using Digital Signal Processing for Electronic Implementation
G. Galeote-Checa, G. Panuccio, B. Linares-Barranco and T. Serrano-Gotarredona

IEEE International Conference on Omni-Layer Intelligent Systems COINS 2021
Adaptación de prácticas de laboratorios de Electrónica y Automatización a una modalidad semipresencial
E. Tena-Sánchez, F.E. Potestad-Ordóñez, M. Valencia-Barrero, A.J. Acosta and C.J. Jiménez-Fernández

Congreso Universitario de Innovación Educativa en las Enseñanzas Técnicas CUIEET 2021
A high-speed low-power sun sensor with solar cells and continuous operation
R. Gomez-Merchan, M. López-Carmona, J.A. Leñero-Bardallo and A. Rodríguez-Vázquez

European Solid-State Circuits Conference ESSCIRC 2021
A Novel Approach for Measurement Throughput Maximization in FPGA-based TDCs
M. Parsakordasiabi, I. Vornicu, A. Rodríguez-Vázquez and R. Carmona-Galán

International Conference on Event-Based Control, Communication and Signal Processing EBCCSP 2021
Novel programmable single pulse generator for producing pulse widths in different time scales
H. Erfanijazi, T. Serrano-Gotarredona and B. Linares-Barranco

International Conference on Content-Based Multimedia Indexing CBMI 2021
Integration of two High-Performance Mixed-Signal Data Conversion IPs
G. Leger, A. Gines, E. Peralias, J.M. Mora and A. Ragel

Int. Workshop on Analogue and Mixed Signal Integrated Circuits For Space Applications AMICSA 2021
Rule Simplification Method based on Covering Indexes for Fuzzy Classifiers
A. Gersnoviez and I. Baturone

IEEE International Conference on Fuzzy Systems FUZZ-IEEE 2021
SoK: Remote Power Analysis
M.C. Martínez-Rodríguez, I.M. Delgado-Lozano and B.B. Brumley

International Conference on Availability, Reliability and Security ARES 2021
Spatial Encoding Techniques in Time-Multiplexed Neural Recording Front-Ends
N. Pérez-Prieto, A. Rodríguez-Vázquez and M. Delgado-Restituto

IEEE International New Circuits and Systems Conference NEWCAS 2021
Simulating the impact of Random Telegraph Noise on integrated circuits
P. Saraza-Canflanca, E. Camacho-Ruiz, R. Castro-Lopez, E. Roca, J. Martin-Martinez, R. Rodriguez, M. Nafria and F.V. Fernandez

Int. Conf. on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design SMACD 2021
Dealing with hierarchical partitioning in bottom-up design methodologies
F. Passos, P. Saraza-Canflanca, R. Castro Lopez, E. Roca and F.V. Fernandez

Int. Conf. on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design SMACD 2021
A study of SRAM PUFs reliability using the Static Noise Margin
E. Camacho-Ruiz, P. Saraza-Canflanca, R. Castro-Lopez, E. Roca, P. Brox and F.V. Fernandez

Int. Conf. on Synthesis, Modeling, Analysis and Simulation Methods and Applications to Circuit Design SMACD 2021
A Real-Time DSP-Based Biohybrid MEA System for Seizure Detection In Vitro
J. Ahmadi-Farsani, D. Caron, G. Panuccio, B. Linares-Barranco and T. Serrano-Gotarredona

IEEE International Symposium on Medical Measurements and Applications MeMeA 2021
On- and Off-centre Pathways in a Retino-Geniculate Spiking Neural Network on SpiNNaker
B.S. Bhattacharya and T. Serrano-Gotarredona

IEEE EMBS Conference on Neural Engineering NER 2021
Cognitive Radio Circuits and Systems - Application to Digitizers
H. Aboushady, A. Sayed, L.A. Camuñas-Mesa and J.M. de la Rosa

IEEE International Symposium on Circuits and Systems ISCAS 2021
Circuit reliability prediction: challenges and solutions for the device time-dependent variability characterization roadblock
M. Nafria, J. Diaz-Fortuny, P. Saraza-Canflanca, J. Martin-Martinez, E. Roca, R. Castro-Lopez, R. Rodriguez, P. Martin-Lloret, A. Toro-Frias, D. Mateo, E. Barajas, X. Aragones and F.V. Fernandez

IEEE Latin America Electron Devices Conference LAEDC 2021
HardBlock: Demonstrator of physically binding an IoT device to a non-fungible token in Ethereum blockchain
J. Arcenegui, R. Arjona and I. Baturone

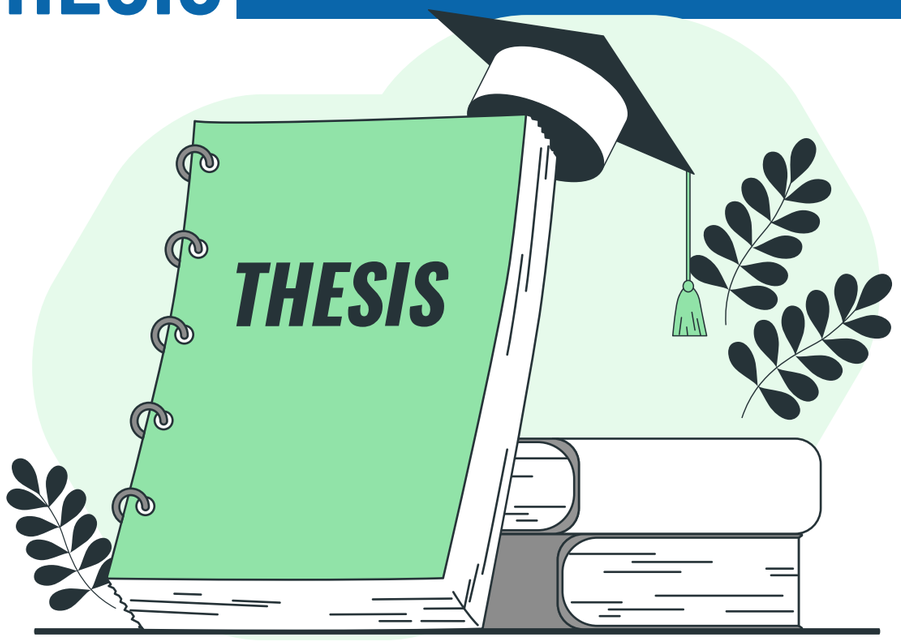
Design, Automation and Test in Europe DATE 2021
A Quantum-Resistant and Fast Secure Boot for IoT Devices using Hash-Based Signatures and SRAM PUFs
R. Román and I. Baturone

EAI International Conference on Safety and Security in Internet of Things SaSeIoT 2021
Low-Power Compensated Modified Comb Decimation Structure for Power-of-Two Decimation Factors
G.J. Dolecek and J.M. de la Rosa

IEEE Latin American Symposium on Circuits and Systems LASCAS 2021
Effects of Electrical Fields on Neuroblastoma (N2A) Cell Differentiation: Preliminary Results
D. Martin-Fernández, P. Pérez-García, M.E. Martín, P. Daza, J.A. Serrano-Viseas, G. Huertas and A. Yúfera

International Conference on Biomedical Electronics and Devices BIODEVICES 2021
Foveal-pit inspired filtering of DVS spike response
S.T.P. Gupta, P. Linares-Serrano, B.S. Bhattacharya and T. Serrano-Gottaredona
Annual Conference on Information Sciences and Systems CISS 2021

THESIS



◆ Memristor Based Event Driven Neuromorphic Nano-CMOS Processor

Charanraj Mohan
Date of defense: February 19, 2021
UNIVERSIDAD DE SEVILLA, IMSE-CNM

◆ Analog-to-Digital Converters for Efficient Portable Devices

Sohail Asghar
Date of defense: March 19, 2021
UNIVERSIDAD DE SEVILLA, IMSE-CNM

◆ Low-Power Artifact-Aware Implantable Neural Recording Microsystems for Brain-Machine Interfaces

Norberto Pérez Prieto
Date of defense: June 30, 2021
UNIVERSIDAD DE SEVILLA, IMSE-CNM

◆ Impacto de la variabilidad dependiente del tiempo en circuitos integrados en tecnologías nanométricas: modelado, simulación y caracterización experimental

Pablo Martín Lloret
Date of defense: September 17, 2021
UNIVERSIDAD DE SEVILLA, IMSE-CNM

◆ Study of variability phenomena on CMOS technolologies for its mitigation and exploitation

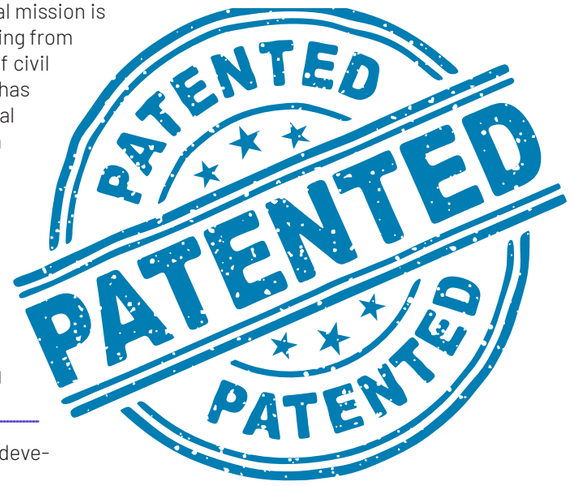
Pablo Sarazá Canflanca
Date of defense: November 12, 2021
UNIVERSIDAD DE SEVILLA, IMSE-CNM

◆ Modeling and simulation of non-linear bioelectronic systems applied to cell culture assays

Juan A. Serrano Viseas
Date of defense: December 10, 2021
UNIVERSIDAD DE SEVILLA, IMSE-CNM

TECHNOLOGICAL TRANSFER

Technology transfer is managed at the Seville Microelectronics Institute by the Projects and Transfer Unit (UPT-IMSE). The UPT's fundamental mission is to promote, channel and manage the ideas and outputs resulting from the research staff's projects into innovations at the service of civil society, the public sector and companies. All our research has the ultimate goal of contributing to generating greater social well-being. For this reason, permanent contact and work with the different economic and social agents is a key pillar in the transversal research carried out at the IMSE. The main objectives of the IMSE Projects and Transfer Unit are:



- ◆ Identify and protect the research results and innovative ideas developed by IMSE research staff.
- ◆ Increase the applicability of investigations by generating permanent contact with interested agents.
- ◆ Establish new technology-based companies that allow the development of the technology that arises.
- ◆ Commercialize and internationalize research in coordination with the CSIC and the University of Seville.
- ◆ Advise the research staff to enhance the industrial application of the results of their projects.
- ◆ Assist the scientific staff to attract financial resources (European, National, regional, and industrial calls).
- ◆ Disseminate information on calls to scientific staff.
- ◆ Advisor on IMSE strategic plans.
- ◆ Attend forums for the dissemination of calls.

PATENTS 2021

New Patent Application in 2021

Electronically foveated dynamic vision sensor

CSIC has developed an electronically foveated dynamic vision sensor that operates at low resolution by default, being able to activate high resolution only when it detects an area of interest. This is a very significant novelty since it allows lower energy consumption, less information and a lower subsequent computational load than a regular dynamic vision sensor

Main innovations and advantages

- In situations in which the visual field observed has a high content of changing information, as occurs during visual capture while driving, it allows non-relevant information to be eliminated and relevant information to be focused, allowing greater detail in capturing what is relevant.
- Allows the reading window to be reduced to the significant relevant area for the analysis, which allows the acquisition speed of the relevant zones to be increased.

- Enables recognition capabilities that can exceed human vision in tasks where multiple regions of interest or attention must be simultaneously addressed, such as real-time surveillance systems, automated driving, or autonomous flight.

Status	Patent pending
Priority	**4/10/21**
Inventors	**Linares Barranco Bernabé; Serrano Gotarredona, María Teresa**
Patent Holder	**Spanish National Research Council and University of Seville**

Low consumption asynchronous solar sensor with photodiodes operating in the photovoltaic región

The low consumption asynchronous solar sensor of the invention falls within the discipline of physical technologies. Particularly, within the area of microelectronic design of optical sensors in standard CMOS technology.
Specifically, a new 10 ultra-low-power, high-speed asynchronous solar sensor architecture for use preferred in space navigation systems. The proposed architecture is adapted to the requirements for the operation of satellites of small size and dimensions that make use of solar sensors to navigate through space, as well as simplifying additional hardware, required in these types of applications.

Main innovations and advantages

- It allows to detect the position of the sun with respect to its centroid.
- Allows you to determine the set of pixels illuminated with a higher level of intensity when there are several sets of illuminated pixels.
- Provides the direction of the centroid of the set of pixels illuminated with the greatest intensity.
- It allows to reduce the time between measurements and avoids extracting data that does not contain information

Status	**Patent pending**
Priority	**4/03/21**
Inventors	**Gómez Merchán, Rubén; Leñero Bardallo, Juan Antonio; Rodríguez Vázquez Ángel**
Patent Holder	**University of Seville and Spanish National Research Council**

Digital OR Pulse Combining Photomultiplier

CSIC and the University of Seville have developed a digital OR pulse combining photomultiplier that reduces unnecessary energy expenditure that occurs in conventional architectures through spatial filtering of spurious avalanches. The technology presented is characterized by being made up of very compact macrocells with high energy efficiency. This allows the design of large digital photomultipliers that work much more efficiently than traditional ones.

Status	**Granted Patent**
Priority	**14/02/2020**
Inventors	**Vornicu, Ion; Carmona Galan, Ricardo; Rodríguez Vázquez, Ángel**
Patent Holder	**University of Seville and Spanish National Research Council**

Detector for measuring electron energy in scanning electron microscopes

CSIC, the University of Cádiz and the University of Seville have developed a detector to measure electron energy in SEM (Scanning Electron Microscope). The detector allows to measure both the intensity and the energy of electrons that are generated in it. This is a very important development. Until now, solid state detectors only measured the intensity of the signal and it was not possible to differentiate whether the changes in the measured signal were due to a change in intensity or to a change in the energy of the incident electrons.

Status	**Granted Patent**
Priority	**01/06/2020**
Inventors	**Carmona Galán, Ricardo and Cervera Gontard, Lionel**
Patent Holder	**Spanish National Research Council, University of Seville and University of Cadix**

EXTERNAL LIAISON

AWARDS & RECOGNITION

Ranking Stanford World's Top 2% cited Scientists

Four IMSE researchers have been listed in Stanford World's Top 2% cited Scientists ranking, which lists the most cited researchers by field. For the IMSE the field is "Electrical and Electronic Engineering". Congratulations to **Ángel Rodríguez Vázquez, José Manuel de la Rosa, Teresa Serrano and Bernabé Linares.** March 10, 2021

First prize in the Entrepreneurship Contest of the Universidad de Sevilla

IMSE predoctoral students **Santiago Fernández and Pablo Pérez** along with IMSE-CNM researchers **Alberto Yúfera, Gloria Huertas and Alberto Olmo**, have won the first prize in the XVI Entrepreneurship Ideas Contest of the Universidad de Sevilla for the best initiative promoted by personnel teacher and researcher. June 2, 2021

EAI SaSeIoT 2021 Best Paper Award

IMSE-CNM researchers **Roberto Román and Iluminada Baturone** have been recipient of the EAI SaSeIoT 2021 Best Paper Award with the work entitled 'A Quantum-Resistant and Fast Secure Boot for IoT Devices using Hash-Based Signatures and SRAM PUFs'.
April 25, 2021

OUTREACH

VISITING IMSE

A visit to the IMSE offers students, teachers, and the public in general an opportunity to obtain first-hand knowledge about the world of research and development in modern microelectronics. Visiting our facilities will certainly be of interest to anyone fascinated by science and technology, and also to those who would like to know exactly what kind of research is carried out in Andalusia and how it is done.

The visit is particularly recommended for high school students and students on professional training courses specializing in science and technology (electronics, IT, etc.).

To visit the IMSE, please contact us

visitas@imse-cnm.csic.es

+34 954 466 666.

TALKS

Microchip designers

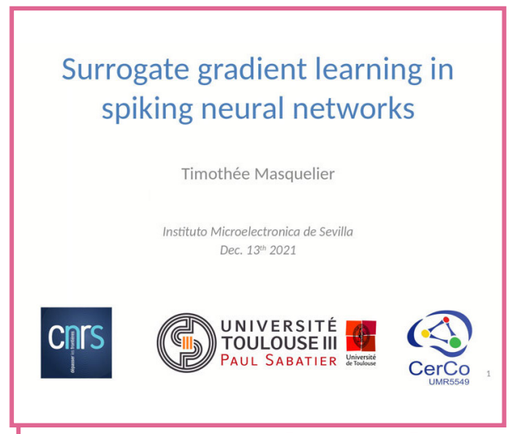
On the occasion of International Women's Day, the IMSE researcher Piedad Brox, gave an online talk entitled 'Microchip Designers' at the Colegio San Agustín in Seville.
March 8, 2021

The Mars Rover Perseverance

Talk by IMSE researcher Servando Espejo Meana entitled 'Mars Rover Perseverance: The challenge of measuring the Martian wind'.
May 12, 2021

The history of chips [image_66]

Talk by IMSE researcher Gloria Huertas in Museo Casa de la Ciencia de Sevilla entitled 'The history of chips' within the cycle 'What do we know about?'
November 19, 2021



Timothée Masquelier [image_67]

Timothée Masquelier, a researcher at the Centre National de la Recherche Scientifique (CNRS), gave a conference on December 13 at the IMSE entitled 'Surrogate gradient learning in spiking neural networks'.
December 13, 2021

EUROPEAN RESEARCHERS' NIGHT

Imse researchers Erica Tena, Francisco Eugenio Potestad and José Miguel Mora presented the activity 'Do you fancy a game? «Frogger» video game reusing programmable boards for microelectronic design'.

September 24, 2021

SOCIAL MEDIA

BLOGS & PRESS HIGHLIGHTS

The technology behind the technology

Interview with Piedad Brox, researcher at the Seville Institute of Microelectronics, about the world of microelectronics, her research work and the projects being developed at the IMSE-CNM.

Source: **Delegación del CSIC en Andalucía y Extremadura**

https://delegacion.andalucia.csic.es/entrevista-a-piedad-brox/

An integrated circuit on Mars... designed in Seville

Something should change in the mentality of those who always see us away from cutting-edge science.

Source: **La Cuadratura del Círculo**

https://www.eldiario.es/andalucia/la-cuadratura-del-circulo/circuito-integrado-marte-disenado-sevilla_132_7226205.html

European SPIRS project

IMSE leads the European SPIRS project. The project will allow Industry 4.0 electronic devices that are connected to a network to increase their security, exchanging information in a secure way and preserving the privacy of those data that are sensitive due to their content.

Source: **Revista CSIC**

From chip to the digital society

Article by professor José Manuel de la Rosa on the platform 'The Conversation', about the impact that the development of microelectronics is producing in our societies.

Source: **The Conversation**

https://theconversation.com/del-chip-a-la-sociedad-digital-165557

Chip shortages: a problem and an opportunity

Article by professor José Manuel de la Rosa on the platform 'The Conversation', about the serious supply problems that the growing demand for chips is causing in various sectors of the industry.

Source: **The Conversation**

https://theconversation.com/desabastecimiento-de-chips-un-problema-y-una-oportunidad-168291

VIDEOS

Memristors, devices that works as memory unit

Intervention by IMSE researcher Bernabé Linares Barranco in the program 'EnRed' of Canal Sur Television.

Source: **Canal Sur Televisión**

https://www.youtube.com/watch?v=heiA-Gy89Rwk

Volum. Heart failure

First prize in the XVI Entrepreneurship Contest of the Universidad de Sevilla

Source: **Universidad de Sevilla**

https://www.youtube.com/watch?v=z4oQH1i-GXoA

SYMAS. Smart Lab: Cell culture monitoring

Finalist in the XVI Entrepreneurship Contest of the Universidad de Sevilla

Source: **Universidad de Sevilla**

https://www.youtube.com/watch?v=SomAl-1Pi3p4

In the frame of EU H2020 MeurONN 'Meet the Expert' series, interview with IMSE Researcher Bernabé Linares-Barranco.

Source: **EU H2020 NEURONN**

https://www.youtube.com/watch?v=l6D1VO-1gWYs

Interview in the frame of EU H2020 NeurONN

In the frame of EU H2020 MeurONN 'Meet the Expert' series, interview with IMSE researcher Maria José Avedillo.

Source: **EU H2020 NEURONN**

https://www.youtube.com/watch?v=bdsLm0KwgGo

The history of chips

Talk by IMSE researcher Gloria Huertas in Museo Casa de la Ciencia de Sevilla entitled 'The history of chips' within the cycle 'What do we know about?'.

Source: **CSIC**

https://www.youtube.com/watch?v=RzyVSKU-YpH8&t

AUDIOS

Passwords that cannot be stolen. SPIRS project

Piedad Brox

Source: **Conectados. Canal Sur Radio**

Book 'De la micro a la nanoelectrónica'

José Manuel de la Rosa

Source: **A tarde. Radio Galega**

Book 'De la micro a la nanoelectrónica'

José Manuel de la Rosa

Source: **De cero al infinito. Onda Cero**

Chips, a non-stock inventory

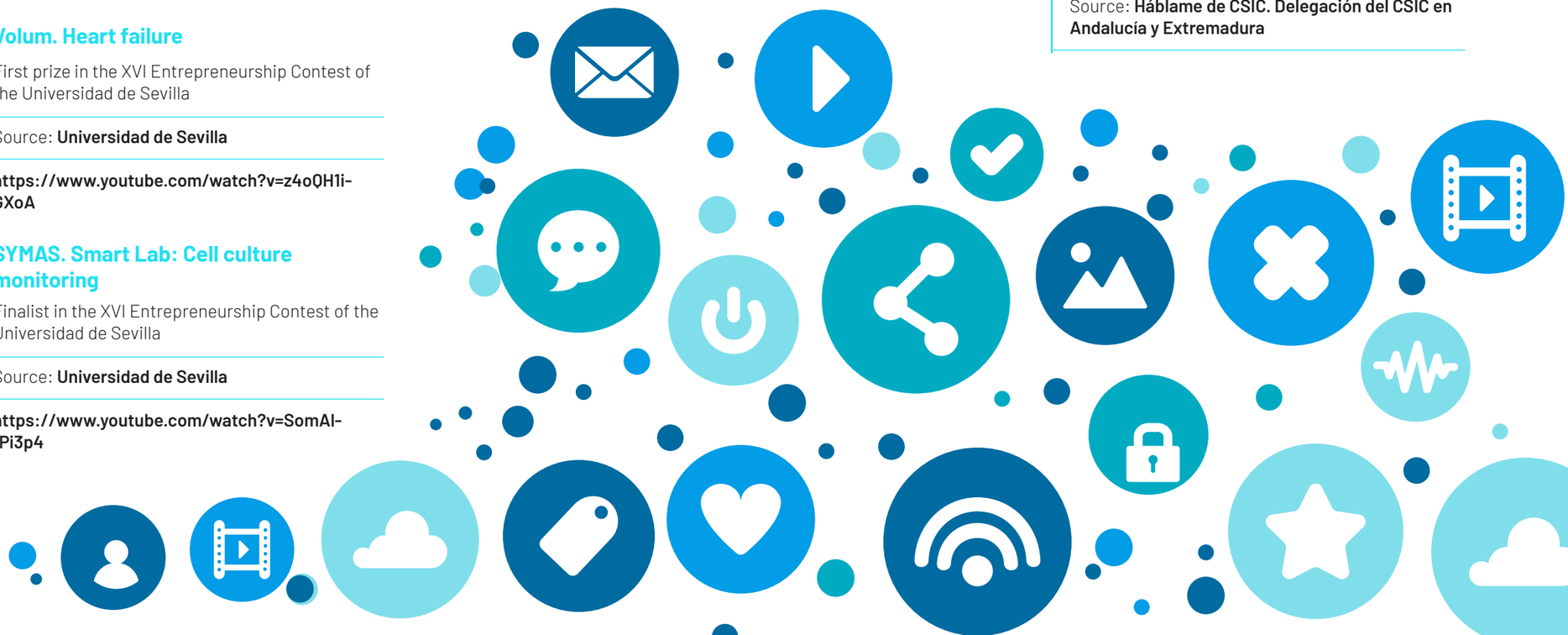
José Manuel de la Rosa

Source: **Puerta al presente. Radio Nacional de España**

SDG 9: 'Industry, innovation and infrastructure'

Bernabé Linares

Source: **Háblame de CSIC. Delegación del CSIC en Andalucía y Extremadura**



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